Comparison of CCM and CRM-based Boost Parallel Active Power Decoupler for PV Microinverter

Yidi Shen, *Student Member, IEEE*, Michael D'Antonio, *Student Member, IEEE*, Shiladri Chakraborty, *Member, IEEE*, Arafat Hasnain, *Student Member, IEEE,* and Alireza Khaligh, *Senior Member, IEEE*

***Abstract*—Single-phase inverter or rectifier systems often make use of an active power decoupler (APD) to balance the mismatch between constant DC power and fluctuating AC power. This manuscript deals with the comparison of continuous conduction mode (CCM) and critical conduction mode (CRM) operation-based design of a parallel boost-type APD for PV microinverter applications. From a design perspective, multi-objective analysis of efficiency, volume, and cost, is explored within a decision space including planar inductors, GaN-based devices, film capacitors, switching frequency, and modulation (CCM vs. CRM). The theoretical study analyzes all possible design configurations within CCM and CRM and identifies Pareto-optimal designs, from which the selected CRM design can achieve reduced system volume and lower cost with the use of smaller inductor core, while operating with similar California Energy Commission (CEC) efficiency drop as the selected CCM design. From a control perspective, a PWM-based control strategy is proposed to implement closed-loop CRM modulation that does not rely on zero-crossing detection (ZCD). Closed-loop systems are designed for the optimal CCM and CRM realizations, and the final system characteristics are compared. Experimental results, obtained using two separate 40 V, 400 W hardware prototypes for CCM and CRM, are presented to verify the analyses.**

***Index Terms*—Microinverter, Active Power Decoupling, GaN switches, CCM, CRM.**

I. Introduction

Single-phase inverters or rectifiers invariably require a low-frequency energy storage mechanism to buffer the instantaneous mismatch between constant DC power and double-line-frequency (DLF) AC power [2]–[4]. The simplest way to achieve this is through the use of capacitors at the DC terminals of the converter. However, most applications like PV inverters and battery chargers have stringent requirements on maintaining low voltage ripple at the DC port. For PV applications, large DC port voltage ripple can significantly reduce the utilization ratio of maximum power, thereby diminishing the harvested energy [5]. For a typical 400 W module-integrated PV microinverter, PV-terminal decoupling would require 2.1 mF and 5.8 mF capacitance to achieve 90% and 98% power utilization ratio respectively. Hence passive decoupling at the converter's dc input would necessitate the use of high-capacitance electrolytic capacitors, which have been widely reported to compromise reliability [6], potentially increasing the PV system levelized cost of energy (LCOE) of the system due to poor lifetime [7]. Furthermore, electrolytic capacitor with high capacitance value for achieving high power utilization ratio may be bulky, adding to the volume of the system and bringing down the power density. An alternate approach is the use of auxiliary active power decoupler (APD) circuits, which employ low-frequency energy buffer capacitors, placed at a different location than the terminal DC port of the converter. This enables wider voltage ripple to exist across the buffer capacitors, leading to reduced capacitance requirement and the use of longer-lifetime film or ceramic capacitors. In general, such auxiliary APD circuits can be placed either at the DC port or the AC port of the main converter, and either in series with or parallel to the main power flow path [3]. This paper specifically deals with the form of APD circuit placed in parallel to the DC port of the main converter, which is henceforth simply referred to as the APD.

Majority of existing literature on different APD topologies [4], [8]–[10] is focused on the design and optimization of high DC voltage ($\sim$400 V) and high-power ($\sim$2 kW) applications, where buck-derived topologies are preferable. In contrast, the analysis in this work specifically focuses on the use of APD in applications with relatively low DC port voltage ($\sim$40 V) like PV microinverter, where a boost-type topology as shown in Fig. 1 is preferable, since the decoupling capacitor has a higher available margin of voltage ripple above the DC port voltage. Such boost-type APD was proposed in [8] and has been investigated with applications in single-phase inverter [4], LED driver [11], and single-phase rectifier [12]. Although the topology has been studied previously, these approaches are mostly based on continuous conduction mode (CCM) operation, which inherently involves hard switching and can lead to unacceptably high switching losses. This can be addressed by the use of critical conduction mode (CRM) operation which enables zero-voltage-switching (ZVS) of the devices, as is done in [13]–[16] for power factor

Part of this paper has been presented at the IEEE PELS sponsored conference ECCE 2020 as reference [1]. The present paper is an extended version with more extensive design space consideration, analysis, details of control implementation, and more comprehensive experimental results.

Yidi Shen, Arafat Hasnain and Alireza Khaligh are with the Department of Electrical and Computer Engineering, Maryland Power Electronics Laboratory, Institute for Systems Research, University of Maryland, College Park, MD - 20742, U.S.A (e-mail: yidishen@umd.edu; hasnain@umd.edu; khaligh@umd.edu.)

Michael D'Antonio was with the Maryland Power Electronics Laboratory (MPEL), University of Maryland, College Park, MD 20742 USA. He is now with SpaceX, 90250, U.S.A (email: mikey.dantonio@gmail.com).

Shiladri Chakraborty was with the Maryland Power Electronics Laboratory (MPEL), University of Maryland, College Park, MD 20742 USA. He is now with IIT Bombay, Mumbai 400076, India (e-mail: shiladri007@gmail.com).

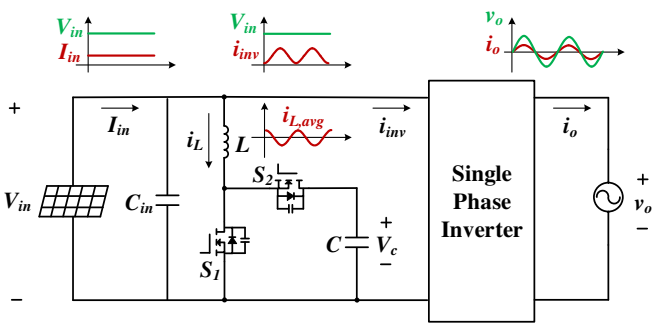


Fig. 1. Topology of the boost-derived parallel active power decoupler (APD).

correction (PFC) rectifiers and in [10], [17] for buck-type APD circuits. Therefore, to design high efficiency, high power-density and low cost inverters in low power applications like PV microinverters, there is a need to comprehensively analyze and explore the feasibility of CRM modulation for boost-type APD in such circuits.

Control strategy of CRM modulation has been discussed widely for PFC rectifier [14]–[16], APD circuit [17], and other power converter circuits with ZVS operation [18]. Time-based hysteretic control strategy, as discussed in [15], is used in all of these CRM circuits. The key functional block in these control circuits is an inductor current zero-crossing-detection (ZCD) module, which is employed to detect the instant when inductor current crosses zero, from which the turn-off and turn-on of the outgoing and incoming switches respectively are triggered after pre-determined time delays with respect to this zero-crossing instant. Though such time-based CRM modulator approaches have been reported before, they are dependent on the accurate realization of the ZCD module, which can be challenging, considering factors like sensor noise and controller delays [19]. Specifically, ZCD can be implemented by employing sense resistor [15], [16], isolated high-frequency current sensor [18], current transformer [19] or saturable inductor [17], which may respectively incur power loss, introduce additional design complexity for auxiliary circuits, and increase cost.

Based on the preceding discussion, the objectives of this paper are twofold. First, a comprehensive multi-objective design comparison is developed for the boost-type parallel APD circuit in the PV microinverter architecture. Specifically, the analysis seeks to compare the two unique CCM- and CRM-based designs across the perspectives of efficiency, volume, and cost. Furthermore, the proposed design framework enables identifications of specific trade-offs in the converter design as a function of the desired performance in the developed objectives. To expand from converter design, the second objective of the manuscript is to compare the CCM- and CRM-based designs from a control perspective. To achieve this, a detailed closed-loop controller design is performed for both the CCM and CRM designs, where a novel pulse width modulation (PWM)-based average inductor current controller is proposed for CRM to eliminate the use of ZCD. In light of the developed design and control perspectives, the manuscript enables holistic comparison of the CCM- and CRM-based boost-type parallel APD circuits, of which experimental results validate the proposed analyses.

The manuscript is ordered as follows: Section II presents the low- and high-frequency principle of operation for the boost APD, following which details of the optimization design and results are presented in Section III. In Section IV, the proposed control strategy for both CCM and CRM is developed and designed. Finally, Section V presents experimental hardware verification results and Section VI concludes the manuscript.

II. Operation Principle of Parallel Boost APD

A. Low-frequency Principle of Operation

The considered boost-derived parallel APD topology is presented in Fig. 1. The switching devices S_1 and S_2 are operated to control the switching-period average of the inductor current, $i_{L,avg}(t) =< i_L(t) >_{T_{sw}}$, to be equal to the 180 degree phase-shifted DLF component of the inverter input current, i_{inv},

$$i_{L,avg}(t) = \left[< i_{inv}(t) >_{2\omega_g}\right] \angle\pi = I_{in}\cos(2\omega_g t) \quad (1)$$

where I_{in} is the DC input current, and ω_g is the grid angular frequency. As such, the input voltage (and hence current) of the PV panel will be DC for maximum power-point tracking.

The APD capacitor, C, is the DLF energy storage component. Modeling the PV input voltage as a fixed DC voltage V_{in} in steady-state, a closed-form expression for $V_C(t)$ is derived using the approach in [10] as,

$$V_C(t) = \sqrt{\frac{V_{in}I_{in}}{\omega_g C}(\sin(2\omega_g t)+1) + V_{C,min}^2}, \quad (2)$$

where $V_{C,min}$ is the minimum value of the capacitor voltage and must be selected to guarantee the boost operation at all times (i.e. $V_{C,min} > V_{in}$).

Setting $sin(2\omega_g t) = 1$ in (2), the maximum voltage can be defined by,

$$V_{C,max} = \sqrt{\frac{2V_{in}I_{in}}{\omega_g C} + V_{C,min}^2}, \quad (3)$$

enabling C to be designed according to the requirements on the range of V_C [2].

B. High-frequency Principle of Operation

The two considered modulation principles, namely CCM and CRM, represent unique design principles and high-frequency switching period operation. A comparison of the two modulation approaches over two example DLF periods is shown in Fig. 2. Due to the AC nature of the inductor current, the APD effectively works in "boost-mode" when $i_{L,avg}(t) > 0$, and in "buck-mode" when $i_{L,avg}(t) < 0$.

1) CCM: In conventional CCM operation presented in Fig. 2(a), the switching frequency is fixed while the duty ratio of S_1 varies according to, $d(t) = 1 - V_{in}/V_C(t)$, to enable tracking of the DLF current. Fig. 2(a) also shows a comparison of inductor current waveforms operating under different switching frequency. As explained in (21) in Appendix A, the current ripple will decrease when the switching frequency increases.

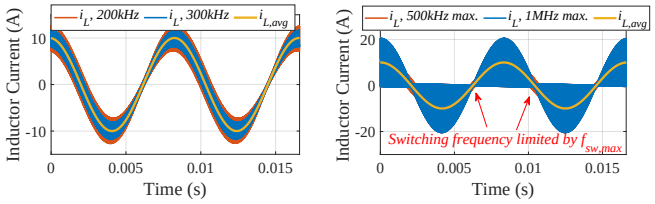


Fig. 2. APD inductor current under different switching frequency parameters and its switching-period-average waveform considering (a) CCM-based control, and (b) CRM-based control.

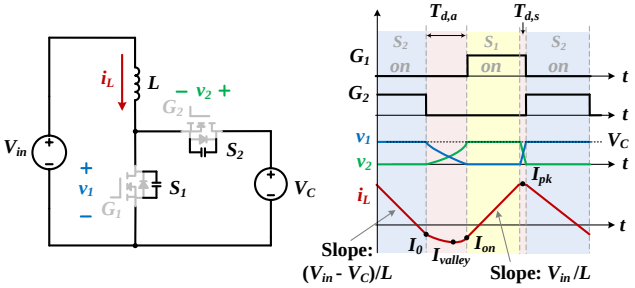


Fig. 3. Equivalent circuit and relevant waveforms of a ZVS transition for S_1 when $i_{L,avg} > 0$ (effective "boost-mode" operation).

Due to continuous conduction operation, the polarity of the inductor current typically does not change during the switching period, except near the average current zero-crossing when low average current values are tracked. Therefore, the usage of CCM modulation results in one device achieving inherent ZVS, while the other is hard-switched in general. Henceforth, the device achieving natural soft-switching[1] is deemed the synchronous device, while the other device is termed the asynchronous device.

2) CRM: In CRM operation presented in Fig. 2(b), the inductor current crosses zero within every switching period, such that ZVS turn-on scenarios are enabled for both devices. The CRM-enabled ZVS turn-on process of S_1 in the positive half cycle ($i_{L,avg}(t) > 0$; effective "boost-mode" operation) is shown in Fig. 3. In this case, S_2 is turned off at inductor current I_0 which reaches a desired negative current threshold. After S_2 turns off, a resonant period ensues between the inductor and the device parasitic output capacitances, with a valley current I_{valley}. If sufficient I_0 (i.e. inductive energy at the initiation of the resonance) and dead-time are provided, S_1 can be turned on with ZVS at its drain-soruce voltage $v_1 = 0$ and inductor current I_on.

While the duty ratio of S_1, $d(t)$ in CRM must remain the same as that in CCM, ZVS across the DLF period in CRM can be facilitated through proper control of the turn-off current I_0 (via the switching frequency), and dead-time. Extension of the ZVS modeling for a half-bridge leg in [20], by analyzing the energy balance in the switching transition, was presented in [1], where the minimum required $I_{0,min}$ can be solved from the constraints on ZVS operation as well as the limit on maximum switching frequency by

$$\begin{cases} \frac{1}{2}LI_{0,min}^2 + Q_{oss}V_C \geq 2Q_{oss}V_{in}, & i_{L,avg} > 0 \\ \frac{1}{2}LI_{0,min}^2 + 2Q_{oss}V_{in} \geq Q_{oss}V_C, & i_{L,avg} < 0 \end{cases} \tag{4}$$

$$|i_{L,avg} + I_0| \left(\frac{1}{V_{in}} + \frac{1}{V_C - V_{in}} \right) \geq \frac{1}{f_{sw,max}}, \tag{5}$$

where Q_{oss} is the charge stored in the device's non-linear output capacitor C_{oss} at V_C, $f_{sw,max}$ is the maximum limit of switching frequency. The impact of $f_{sw,max}$ on the inductor current waveform is shown in Fig. 2(b), where generally only the inductor current ripple near the zero-crossing is affected as the maximum decreases (i.e. the current ripple and duration of frequency clamping increases).

In addition to ensuring proper minimum turn-off current to guarantee ZVS through the use of variable switching frequency, the device dead-time must also be accurately set. The minimum required dead-time can be calculated by,

$$t_{ZVS} = \int_0^{V_C} \frac{C_x(v)dv}{\sqrt{I_0^2 + \frac{2}{L}\int_{\gamma V_C}^{v} C_x(v_x)(V_{in} - v_x)dv_x}}, \tag{6}$$

where $\gamma = \{1, i_{L,avg} > 0;\ 0, i_{L,avg} < 0\}$, I_0 is the switching instant current, and $C_x(v) = C_{oss}(v) + C_{oss}(V_C - v)$ is the switch-node equivalent capacitance, as the output capacitances of S_1 and S_2 are effectively connected in parallel [21].

III. Multi-objective Design Comparison

Multi-objective design analysis regarding efficiency, power density, and cost, is conducted for the APD within a 40 V, 400 W, microinverter system to inform parametric design decisions and component selection. While the proposed design framework enables the identification of optimal design configurations within the target objectives, the analysis is extended to explore trade-offs within the decision space corresponding to their respective impact on the objective space.

A. Decision Space

A block diagram of the multi-objective optimization procedure is shown in the top inset of Fig. 4. It is clear that the decision space is composed of five components, namely the selected device, inductor, APD base capacitor, number of capacitors in parallel, and the switching frequency (specifying the fixed value in CCM versus the maximum limit for CRM).

1) Inductor database and switching frequency: The decision space for the APD inductors was composed of pre-designed planar-based configurations with varying core geometry (specifically ER-based geometries from Ferroxcube with 3F36 material), number of turns, and air-gap lengths. The range of the considered inductance was considered in tandem with the decision space of the switching frequency. Specifically for CCM, inductance and frequency were determined according to the inductor current ripple consideration,

[1]Natural soft-switching refers to the switching transition of the device that undergoes ZVS turn-on for CCM operation, that is S_2 in "boost-mode" and S_1 in "buck-mode".

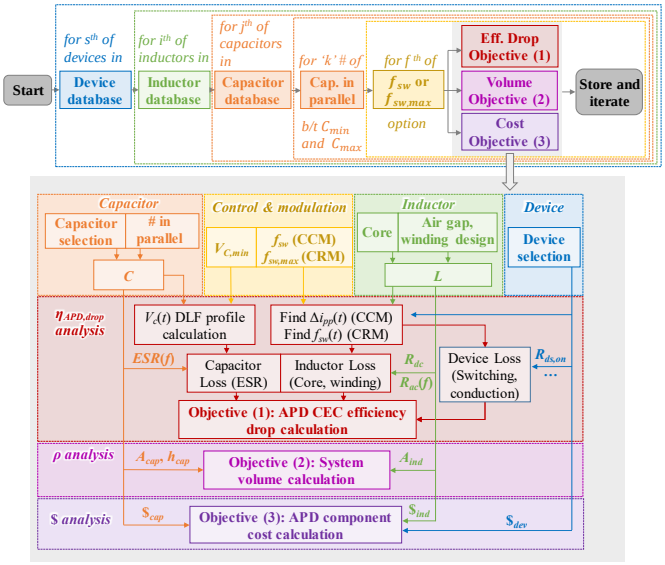


Fig. 4. Block diagram explaining the multi-objective optimization process.

TABLE I
OPERATING SPECIFICATIONS, COMPONENT SELECTION, AND DECISION SPACE OF THE OPTIMAL DESIGN ANALYSIS FOR CCM AND CRM.

Design Variable		CCM	CRM
Input Voltage		40 V	
Input Power		400 W (full power)	
Switch		EPC2010C, EPC2215, EPC2059 EPC2034C, EPC2033, EPC2207	
Capacitor		160 V KEMET R60 series, 6.8 - 68 μF Total C = C_{min} – $2C_{min}$	
Inductor	Inductance	20 - 70 μH ($\Delta I_{pp} < 15$ A)	2 - 10 μH ($f_{sw,min} \in [100, 500]$kHz)
	Core Geometry	ER51/10/38 ER41/7.6/32 ER32/6/25	ER32/6/25 ER23/3.6/13 ER18/3/10
	Design Criteria	Turns $N \in [4, 14]$ Core material: 3F36 Winding: 4 layer planar 3 oz copper Maximum flux density $B_{max} \in [300, 350]$ mT	
Switching Frequency [kHz]		$f_{sw} \in [100, 300]$	$f_{sw,max} \in [500, 1000]$
$V_{C,min}$*		45 V	
* denotes pre-selected components			

where a maximum peak-to-peak current $\Delta I_{pp} < 15$ A was enforced. On the other hand for CRM, the inductances were selected to limit the minimum switching frequency between $f_{sw,min} \in [100, 500]$ kHz. All of the considered inductor designs within the decision space were analyzed using 3D FEA simulations in Ansys Maxwell to create a database of inductance, DC resistance and AC resistance as a function of frequency, which were then used in the inductor loss estimation.

2) Device database: Six different GaN-based switching devices from EPC were considered, each with unique rated voltage (> 150 V) and current (> 15 A). As a result of the different voltage and current ratings, unique characteristics of output capacitance C_{oss}, on-state drain-source resistance $R_{ds,on}$, and cost are realized across the decision space of the devices. Importantly, the selection of device has a direct impact on the minimum APD capacitance, according to a rearrangement of (3) shown as

$$C_{min} = \frac{2V_{in}I_{in}}{\omega_g \left(V_{C,max}^2 - V_{C,min}^2\right)} \tag{7}$$

where a 40% margin below the rated device voltage (i.e. $V_{C,max} = V_r/\ 1.4$) was considered for the maximum capacitor voltage, $V_{C,min} = V_{in} + 5V$ was selected to ensure the boost operation of APD, and maximum input power $V_{in}I_{in}$ was used to find the minimum required C at the worst operation cases.

While Si-based devices could also be considered, specifically GaN-based devices were selected in the decision space for their enhanced performance in efficiency and increasing cost-effectiveness [22].

3) Capacitor database: Considering dissipation factor and lifetime, the KEMET R60 series film capacitors with a 160 V DC voltage rating were selected as the base capacitors in the proposed design. Specifically, a range of C_{base} = 6.8 to 68 μF was considered, where each capacitor has unique dimensions and cost. To realize the total APD capacitance bank multiple base capacitors are considered to be connected in parallel. Importantly, only a lower bound exists for the total capacitance bank, found as a function of the selected switching devices in accordance with (7), hence the number of capacitors in parallel (deemed n_{cap}) is an additional free design variable. Specifically, the number of capacitors in parallel is selected such that the total capacitor bank is between $C \in [C_{min}, 2C_{min}]$.

B. Optimization Procedure

As shown in Fig. 4, five nested loops are run to analyze all possible combinations for each selection in the device database, each selection in the inductor design database, each selection in the capacitor database, each possible number of capacitors in parallel, and each selection of switching frequency for the decision space summarized in Table I. For each given design configuration, three objective functions representing the performance in efficiency, volume, and cost, are calculated and stored for further analysis. The algorithm proceeds in an iterative fashion until the analysis over all possible combinations are completed.

1) Efficiency drop: For the efficiency prediction, a comprehensive loss model is developed for the APD considering device losses (namely switching loss, on-state conduction loss and reverse conduction loss), inductor losses (namely core and conduction loss), and APD capacitor equivalent-series-resistance (ESR) loss. Regarding the efficiency drop calculation, for each design configuration the trajectory of the APD capacitor voltage across the DLF period is determined with (2) according to the total capacitance (i.e. $C = n_{cap} \cdot C_{base}$) and the pre-selected minimum capacitor voltage $V_{C,min}$. Additionally, the switching period profile of the high-frequency inductor current across the DLF period is calculated according to the inductance, device characteristics, and switching frequency (in CCM) or the soft-switching requirement (in CRM via (4)), with specific calculations for inductor RMS current $I_{L,rms}$

and ΔI_{pp} provided in the Appendix. Finally, the profiles of capacitor voltage and inductor current are distributed to unique loss model blocks for the calculation of losses in each component, where the detailed loss calculation procedure is discussed in detail in the Appendix.

With the loss model and operation analysis, the total APD power losses can be calculated for each switching period, and averaged across the DLF period. As the APD is connected in parallel to the main inverter circuit, the total microinverter circuit loss is the sum of the losses in the APD and the main inverter stage. To quantify the efficiency-related performance of the APD circuit, a factor deemed the APD efficiency drop ($\eta_{APD,drop}$) is introduced, which denotes the net decrease in microinverter efficiency due to the addition of the APD. At a given power level P_{in}, this factor is given by,

$$\eta_{APD,drop} = P_{APD,loss}/P_{in}, \tag{8}$$

where $P_{APD,loss}$ is the average of the losses in the APD across the DLF period.

In microinverter systems, weighted efficiency metrics such as the California Energy Commission (CEC) efficiency which is standardized in [23], based on irradiance and temperature data representative of Southwest US (California area), are of particular significance. The APD efficiency drop at a given power level can be extended to define the APD CEC efficiency drop, calculated by,

$$Y(1) = \eta_{CEC,drop} = \sum_{i=1}^{6} C_i \cdot \eta_{APD,drop-i}, \tag{9}$$

where the weighting coefficients are $C = \{C_i\} = \{0.04, 0.05, 0.12, 0.21, 0.53, 0.05\}$, $\eta_{APD,drop-i}$ is the APD efficiency drop under the power levels of interest $P_{in} = \{10\%, 20\%, 30\%, 50\%, 75\%, 100\%\}P_{max}$, where $i = 1, 2, ...6$ [23]. As indicated, the APD CEC efficiency drop is utilized as the first objective function Y(1) to be minimized, of which designs with low efficiency drop are beneficial to the system from a loss perspective.

2) System Volume: To evaluate the performance of the evaluated APD designs from a power density perspective, a simple volume model is developed. From a manufacturing perspective, it is considered that surface mount components are located on the top-side of the printed-circuit-board (PCB), while through-hole components are placed on the bottom-side of the PCB. Furthermore, since the APD does not work in isolation, but always in conjunction with the main inverter circuit, the area of the inverter circuit (henceforth A_{inv} = 169 cm^2) must also be considered. This is especially true for the proposed design, where the main-circuit and APD are designed on a single PCB for cost-effectiveness. In light of these two points, four key assumptions are taken in the APD volume calculation: 1) no APD top-side component will be taller than the main-circuit inverter top-side height h_{top} = 7 mm; 2) no other bottom-side component will be taller than the APD capacitor (on the bottom-side as it is a through-hole component); 3) with the capacitors mounted on the bottom-side, the top-side area above can be used for sensors, devices, and gate driving circuitry, such that the corresponding component area need not be included; and 4) component placement and routing is ideal such that no additional space is wasted. With the proposed assumptions in mind, only the APD inductor and capacitor will contribute to the APD footprint area. Therefore, considering a specific inductor design, capacitor, and number of capacitors in parallel, the second objective function describing the full inverter system volume can be calculated by,

$$Y(2) = V_{sys} = (A_{ind} + n_{cap}A_{cap} + A_{inv})(h_{top} + h_{cap}) \tag{10}$$

where A_{ind} is the inductor footprint area, A_{cap} is the capacitor footprint area, and h_{cap} is the APD capacitor height.

3) Component Cost: The third objective function is defined as the total APD component cost calculated by,

$$Y(3) = cost_{APD} = 2cost_{dev} + cost_{ind} + n_{cap}cost_{cap}, \tag{11}$$

based on distributor component pricing at quantities $\approx$ 1,000, to enable a one-to-one comparison. Aside from the device, inductor, and capacitors, non-design-dependent components including the gate driver, sensors, and other auxiliary circuitry, are not considered.

C. Comparison of Results - CCM vs. CRM

All combinations of decision space variables from Table I were stored and evaluated for their performance across the CEC efficiency drop, system volume, and cost objectives, in coordination with the block diagram in Fig. 4. The results of the analysis with all design configurations mapped to the 3D objective space are shown in Fig. 5(a)-(b) for CCM and CRM, respectively. According to the multi-objective optimization theory, Pareto-optimal designs correspond to non-dominated configurations in the objective space, where dominated configurations can be defined between any two pair-wise points as [24]: Y_1 dominates Y_2 if both of the following conditions are satisfied [2],

$$\text{i) } Y_1(i) \leq Y_2(i) \forall i \in o, \tag{12a}$$

$$\text{ii) } \exists i \in o \text{ s.t. } Y_1(i) < Y_2(i), \tag{12b}$$

where o is the numbered set of objective functions. The Pareto-optimal designs can extracted from the objective space by comparing every pair of feasible design points across the two guidelines in (12). Design points which are dominated are excluded from the Pareto-optimal set. Following application of (12) to every pair of feasible design points, the remaining design points are non-dominated and hence constitute the Pareto-optimal set, meaning that no other design point simultaneously achieves lower volume, lower CEC efficiency drop, and lower cost. Design points in the Pareto-optimal set are shown in Fig. 5(a)-(b) for CCM and CRM, respectively, with a larger scatter size and black outline.

[2]Here all objective functions are assumed to be minimized, as is consistent with the present APD design problem. For a general case, analogous formulations can be used [24].

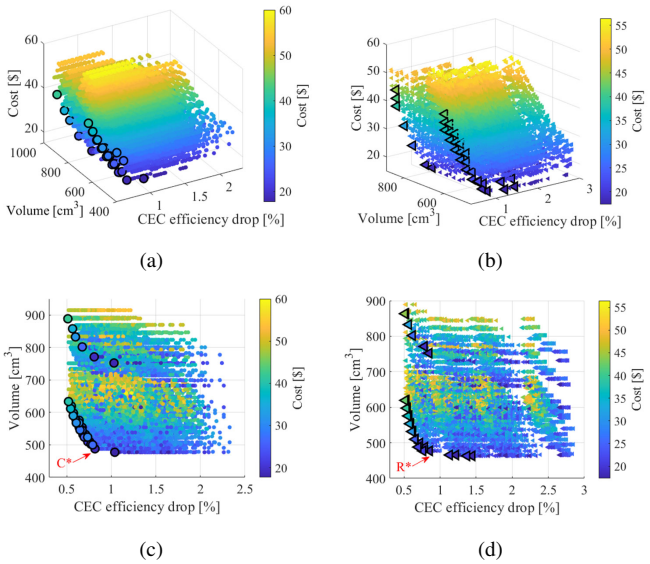


Fig. 5. 3D plot of the multi-objective optimization results of the CEC efficiency drop, system volume and cost for (a) CCM, and (b) CRM, and 2D plot of the multi-objective optimization results of the CEC efficiency drop and system volume for (c) CCM, and (d) CRM, cost is represented by color. Design points in Pareto-optimal set are indicated with larger size and black outline. Selected optimal designs for CCM and CRM are indicated as C* and R*, respectively.

In the Pareto-optimal set for CCM and CRM, the trade-off between efficiency, power density, and cost, should be considered to select the proper designs according to the target and priority across the different objectives. In the proposed 400 W microinverter design case, cost is prioritized as the most significant design objective, while efficiency drop and volume shall at least meet a pre-defined maximum design target. Specifically, designs with volume <600 cm^3 and CEC efficiency drop <1% are deemed acceptable. To better visualize the performance of the Pareto-optimal designs according to the proposed design targets, 2D objective space plots for volume versus efficiency drop (with the cost shown by the color of the scatter fill) are shown in Fig. 5(c)-(d), respectively. Based on the observed trade-offs, optimal designs are selected for the minimum cost among points where the volume and efficiency targets are satisfied, ensuring fair performance across all three objective functions. In Fig. 5(c)-(d), C* and R* are used to indicate the selected optimal design point for CCM and CRM, respectively.

Specifications of the selected C* and R* designs are listed in Table II. It is shown that the optimal design for CCM and CRM are achieved with the same device (EPC2207) and the same capacitor (four $24\times41.5\times15$ mm 33 μF capacitors in parallel), while the inductor in CRM can be achieved by a smaller core (ER32/6/25) compared to CCM (ER41/7.6/32). In light of the unique core selection, design R* inherits both lower volume ($\sim$10 cm^3 lower) and lower cost ($\sim$\$0.7), while the CEC efficiency drop is very close (<0.1% difference). A further breakdown of the CEC efficiency drop by loss mechanism for the C* and R* designs is presented in Fig. 6. It is evident that CRM effectively eliminates the switching loss by realizing full ZVS of both devices throughout the DLF period. However,

TABLE II
DESIGN PARAMETERS OF OPTIMAL DESIGN CASES FOR CCM AND CRM.

Design Parameter	CCM	CRM
Device	EPC2207	
Inductor Core	ER41/7.6/32	ER32/6/25
Inductor Footprint Area	1301 mm^2	815.3 mm^2
Air Gap Length L_g	226 μm	354 μm
Turns N	4	4
Inductance L	22.2 μH	9.8 μH
Capacitor	33μF (24 $\times$ 41.5 $\times$ 15 mm)$\times$3	
Switching Frequency (CCM)	f_{sw} = 200 kHz	-
Maximum Switching Frequency (CRM)	-	1 MHz
Predicted CEC Efficiency Drop	0.82%	0.85%
System volume	487.97 cm^3	477.30 cm^3
Cost	\$ 18.41	\$ 17.70

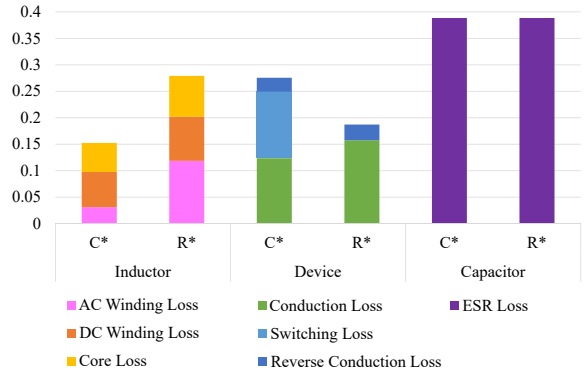


Fig. 6. CEC efficiency drop comparison between unique loss mechanisms of the selected CCM and CRM optimal designs from Table II

most conduction losses, aside from the APD capacitor ESR loss, increase in CRM due to the significantly pronounced current ripple. In particular, the inductor AC winding loss and core loss increased significantly in CRM as compared to CCM.

D. Decision Space Trade-offs

To demonstrate the effectiveness of the optimal designs C* and R* as well as understand how the selection of each design parameter in the decision space impacts the objective functions, C* and R* are evaluated with variation in one design variable at a time, keeping all other variables at their optimal values listed in Table II.

1) Impact of Device: Performance of the C* and R* designs with variation in the switch selection (between only the 200 V devices) are compared in Fig.7(a)-(b), respectively. In particular, analysis is only presented for cost versus efficiency drop, as the device selection does not contribute to the system volume calculation. It is clear in Fig.7(a) that the C* design with EPC2207 (identified with red text) inherits both the lowest cost and lowest CEC efficiency drop, mainly due to the reduction of hard switching loss resulting from the low output capacitance of the device. On the other hand, results for CRM in Fig.7(b) highlight that lower on-state resistance devices including the EPC2215 and EPC2034C are advantageous from the perspective of CEC efficiency drop, as the devices only exhibit conduction-related losses. However, these devices are

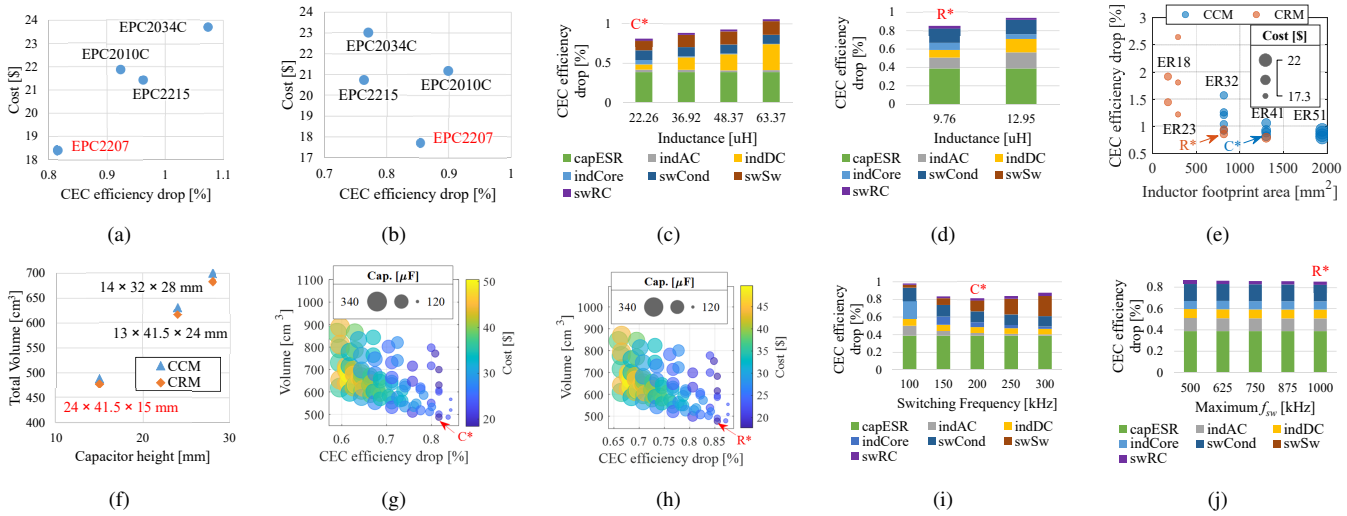


Fig. 7. Comparison of the C* and R* designs with single parameter variation. CEC efficiency drop versus cost for designs with unique 200 V devices in (a) CCM, and (b) CRM; CEC efficiency drop breakdown by loss mechanism versus inductance considering the fixed core geometry (c) ER41/7.6/32 in CCM, and (d) ER32/6/25 in CRM; (e) CEC efficiency drop and cost versus inductor footprint area for designs with unique inductor core geometries; (f) system volume versus capacitor height for designs with unique capacitor dimensions within the same 33μF base capacitance; CEC efficiency drop, system volume, and cost, for designs with unique capacitor selections in (g) CCM, and (h) CRM; and CEC efficiency drop breakdown by loss mechanism versus switching frequency for (i) CCM, and (j) CRM.

more expensive than the EPC2207, where in particular the benefit of a slight reduction in CEC efficiency drop ($\approx 0.1\%$) was not substantiated for the increase in system cost ($\approx$ 3$; a 17% penalty). Nevertheless, in applications for which cost is not a priority, the selection of the EPC2215 device in CRM would have inherent performance advantages.

2) Impact of inductor: Evaluation of the C* and R* designs with variation in the inductor is compared in Fig. 7(c)-(e). Within the inductor decision space, inductor designs include variation in core geometry and inductance (via the number of turns and air-gap length), where the only variation in core geometry will affect the volume and cost of the design. Therefore, the impact of the inductor design can be split into two analyses, first for inductor designs with the same core footprint and second across inductor designs with varying core footprints.

For a given inductor core geometry, design variations in the turns and air gap only affect the efficiency objective. Fig. 7(c)-(d) shows the comparison of CEC efficiency drop by loss mechanism in the C* and R* configurations, respectively, with varying inductance values achieved with the same core (i.e. ER41 for C* and ER32 for R*). In CCM, the inductor DC winding loss in yellow increases for higher inductances due to more turns, and hence higher DC resistance, while core loss and conduction loss decreases due to reduced inductor current ripple. Similarly in CRM, the inductor DC and AC winding losses increase for higher inductance, again due to more turns and higher resistances, while core losses decrease due to lower switching frequency. In either case, it is clear that the selected designs C* and R* are optimal among designs with different inductances due to inheriting minimum CEC efficiency drops.

When the core size varies, the system volume and cost will also vary due to the different core footprint area and price of the core. In Fig. 7(e), CEC efficiency drop is plotted versus the inductor footprint area (with cost represented by the size of the scatter points), with all other parameters the same as C* and R*. It is clear that, the use of a larger inductor core can achieve lower efficiency drops, as the inductor windings can be wider reducing the effective DC and AC resistances. However, both volume and cost will directly increase with the increase of core size, hence the selection of the core can be determined by the system-level trade-off between efficiency and core size. Under the proposed design targets discussed in the previous section, design C* and R* were selected due to achieving the smaller core size, and hence core cost, while meeting the CEC efficiency drop target of $<1\%$.

3) Impact of capacitor: Selection of the APD capacitor, and number of capacitors in parallel, will have the most pronounced effect to efficiency drop (due to non-negligible low-frequency ESR loss), volume (due to the large capacitor area and height), and cost. As indicated in Table II, four 33 μF capacitors in parallel were selected for optimal designs C* and R*. Within the 33 μF base capacitor, three unique geometric configurations were available, of which the total system volume versus capacitor height is shown in Fig. 7(f). It is clear that while achieving the same efficiency drop (as the capacitance and dissipation factor is the same across these capacitors) and cost, the system volume is minimized for the largest area but lowest height capacitor indicated in red text. As the capacitor is the tallest component on the bottom-side of the microinverter system, deciding the form factor of the converter on the bottom-side, minimization of the capacitor height is more important than minimization of the capacitor area.

It is worth noting that the selection of the optimal capacitor dimension is dependent on the considered area of microinverter main circuit. Although only the APD circuit is designed in the proposed multi-objective analysis, the area of

TABLE III
COMPARISON BETWEEN OPTIMAL DESIGNS WITH VARIATION IN THE VOLUME OBJECTIVE FUNCTION DEFINITION. NOTE: * = SYSTEM; ' = APD

Design Parameter	CCM		CRM	
Design Number	C*	C'	R*	R'
Capacitance	33μF×3			
Area Dim. [mm]	24×41.5	13×41.5	24×41.5	14×32
Height [mm]	15	24	15	28
System volume [cm^3]	487.97	630.99	477.30	682.62
APD volume [cm^3]	116.26	107.21	105.59	91.26
Expected $\eta_{CEC,drop}$	0.82 %		0.85 %	
Cost	\$18.41		\$17.70	

inverter circuit was specifically included in the volume model in (10). On the other hand, if the APD design is performed standalone without considering the inverter main circuit, a different volume model can be considered as

$$V_{APD} = (A_{ind} + n_{cap}A_{cap})(h_{top} + h_{cap})\cdot \qquad (13)$$

Considering (13) as the volume-related objective function, the optimization can be re-iterated, where the corresponding optimal design configurations, deemed C' and R' for CCM and CRM, respectively, are compared against C* and R* in Table III. Interestingly, minimizing only the APD-related volume leads to selection of the capacitor with the smallest footprint area and largest height. It is evident that corresponding to the increase of in inverter circuit area, the height determined by the APD capacitor impacts the power density over a larger area, encouraging the selection of shorter capacitors. Therefore, since the APD is not operated standalone in the application, the area of inverter main circuit is significant to consider in the optimal component selection of APD and should be taken into consideration.

On another note, Fig. 7(g)-(h) highlights performance of the C* and R* designs across all three objective functions with unique base capacitors and number of capacitors in parallel. As the total decoupling capacitance increases, the capacitor ESR reduces that enables a reduction in the CEC efficiency drop. Furthermore, the hard switching loss in CCM also reduces when the capacitance increases, due to the reduced effective range of the capacitor voltage. However, larger capacitance and more capacitors in parallel contribute significantly to increases in system volume and cost. In the proposed application, designs C* and R* are optimal due to the low cost and system volume while achieving a CEC efficiency drop $<1\%$.

4) Impact of switching frequency: Variation of switching frequency and the corresponding impact to efficiency are compared in Fig. 7(i)-(j) for C* and R*, respectively. For CCM, the CEC efficiency drop breakdown by loss mechanism versus switching frequency is plotted in Fig. 7(i). With the increase of switching frequency, switching loss increases, while AC winding loss and core loss decrease due to the reduction in inductor current ripple (cf. Fig. 2(a)). For a given design, a unique minimum in CEC efficiency drop will exist as a function of frequency, of which f_{sw}= 200 kHz is optimal for the C* design. For CRM, CEC efficiency drop breakdown by loss mechanism versus maximum switching frequency is plotted in Fig. 7(j). The change in efficiency drop is not as significant in this case, as the only operating points affected by the maximum frequency bound are low average current points, as shown in Fig. 2(b). According to Fig. 7(j) the CEC efficiency drop finds its minimum at maximum switching frequency 1 MHz for the optimal design R*, though the sensitivity is small.

IV. CONTROL IMPLEMENTATION

A. Control Strategy Comparison - CCM vs. CRM

To achieve APD operation, the average inductor current needs to be controlled to follow a sinusoidal reference current, such that the sum of the APD current and inverter current is a flat DC current. In general, a current controller can be used to derive the duty cycle for the complementary switching devices, as the average inductor current is controlled to track a provided reference, coresponding to the DLF component of single-phase inverter DC-side current.

PWM-based average inductor current control strategy, as shown in Fig. 8(a), is commonly used in CCM due to its direct control to average inductor current. The sensed inductor current is first passed through an analog low-pass-filter (LPF) to attenuate the switching frequency components in the inductor current, returning only the switching-period-average $i_{L,avg}$. The average inductor current is then compared to the current reference, and the error is controlled to zero with a proportional–integral (PI) controller. The output of the PI controller is the S_1 duty ratio, d, which can be converted to the gate drive signal of the two devices by a PWM block, where the pulse-width is modulated by comparing d to a switching frequency carrier waveform.

Conventionally, time-based hysteretic current controller with ZCD is used in CRM-based circuits [25], of which an example structure is shown in Fig. 8(b). A ZCD module is required to detect the inductor current zero-crossing instant, inherently guaranteeing a ZVS condition for the asynchronous device. The synchronous device can be controlled to turn off after the inductor current crosses zero and reaches a desired I_0 value to ensure the ZVS turn-on of the asynchronous device. On this basis, predictive or closed-loop $i_{L,avg}$ control module will trigger the other switching transition instants when the switching period average current $i_{L,avg}$ reaches the reference value. Thus, all the turn-on and turn-off signals can be generated from the delay of ZCD signal.

The PWM-based average inductor current control strategy is specifically suitable for CCM APD due to the simple implementation, where the switching frequency and dead-time are fixed. An adaption of the PWM-based average current control for use in CRM is proposed in this manuscript, which facilitates variable switching period and dead-time through the introduction of look-up-table (LUT) or dynamic calculation blocks. As described in Section II-B2, dynamic variation of the switching period and dead-time (dependent on the operating point, namely average inductor current $i_{L,avg}$, input voltage V_{in}, and APD capacitor voltage V_C) are critical to guarantee ZVS of the asynchronous device. By adopting predictive

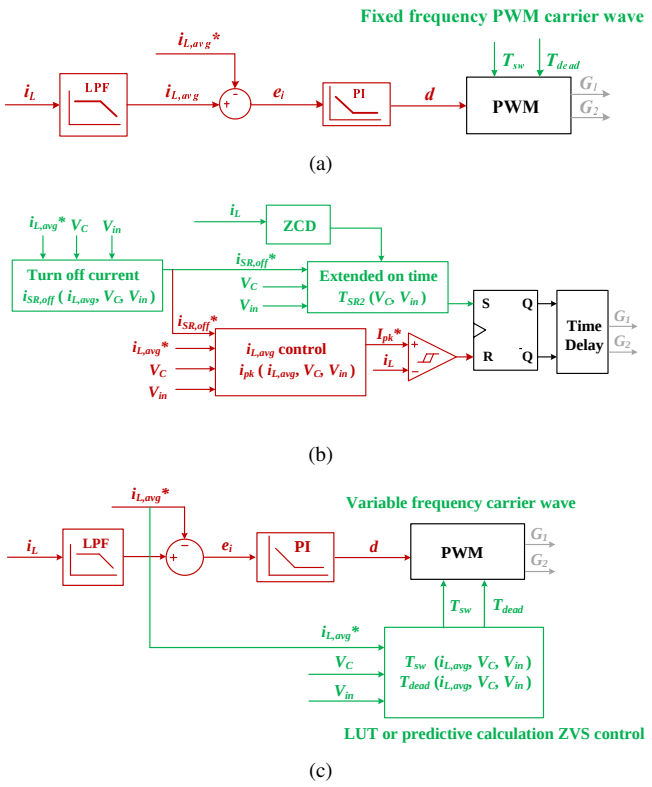


Fig. 8. Block diagram of (a) PWM-based average current controller for CCM, (b) Time-based hysteretic current controller with ZCD [15], where definition and calculation of synchronous rectifier device turn off current $i_{SR,off}$ and extended turn on time after zero-crossing T_{SR2} can be found in [15], and (c) proposed PWM-based average current controller for CRM.

switching period control, the conventionally used ZCD module and corresponding auxiliary circuits can be eliminated.

B. Predictive Equations for Proposed CRM Modulator

For the proposed CRM control strategy, predictive equations for the switching period and dead time must be derived. The switching period can be calculated based on the operation principle and transition analysis in Section II-B2, combined with the detailed inductor current profile in Fig. 3, via

$$T_{sw} = \begin{cases} \dfrac{(I_{pk}-I_0)L}{V_{in}} + \dfrac{(I_{pk}-I_{on})L}{V_C-V_{in}} + T_d, & i_{L,avg} > 0 \\ \dfrac{|I_{pk}-I_{on}|\,L}{V_{in}} + \dfrac{|I_{pk}-I_0|\,L}{V_C-V_{in}} + T_d, & i_{L,avg} < 0 \end{cases} \tag{14}$$

with knowledge of the desired turn-off current of the synchronous device, I_0, turn-on current of asynchronous device I_{on}, the peak current I_{pk}, and total dead-time $T_d = T_{d,a} + T_{d,s}$, where $T_{d,a}$ and $T_{d,s}$ refer to the dead time before turn-on of the asynchronous and synchronous devices, respectively[3]

The turn-off current of the synchronous device, I_0, should have an absolute value greater than the minimum ZVS and $f_{sw,max}$ boundary current, $I_{0,min}$, calculated with (4) and (5). With I_0 determined, the asynchronous device turn-on current I_{on} can be solved according to the energy balance criteria of the ZVS transition,

$$\begin{cases} \dfrac{1}{2}LI_0^2 + Q_{oss}V_C = 2Q_{oss}V_{in} + \dfrac{1}{2}LI_{on}^2, & i_{L,avg} > 0 \\ \dfrac{1}{2}LI_0^2 + 2Q_{oss}V_{in} = Q_{oss}V_C + \dfrac{1}{2}LI_{on}^2, & i_{L,avg} < 0 \end{cases} \tag{15}$$

Finally, the peak current can be estimated by $I_{pk} = 2i_{L,avg} - I_{valley}$ [15]. In particular, I_{valley} can be determined by

$$\begin{cases} L(I_{valley}^2 - I_0^2) = 2(V_C - V_{in})^2 C_{eq,Q}, & i_{L,avg} > 0 \\ L(I_{valley}^2 - I_0^2) = 2V_{in}^2 C_{eq,Q}, & i_{L,avg} < 0 \end{cases} \tag{16}$$

where the device output capacitance can be modeled as a fixed charge-equivalent capacitance, $C_{eq,Q} = Q_{oss}/V_C$ [21].

In addition, the predictive dead time calculation should control the dead time to be the required ZVS time according to the turn-off current as $T_{dead} = t_{zvs}$, so that ZVS can be achieved and reverse conduction loss can be minimized.

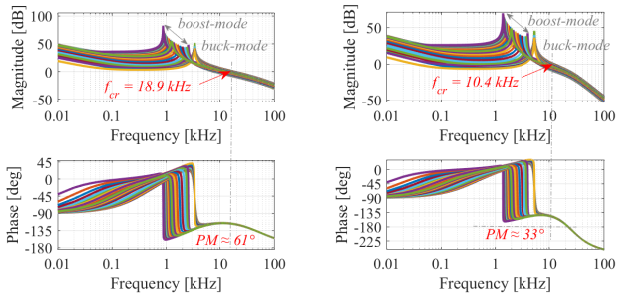
From (6) and (14)-(16), predictive determination of the switching period and dead-time can be calculated from the desired $i_{L,avg}$, sensed V_{in}, and sensed V_C. The predictive equation set module can be realized by offline pre-calculated LUTs stored in the DSP. However, as both T_{sw} and $T_{d,a}$ are functions of $i_{L,avg}$, V_{in}, and V_C, three-dimensional LUTs are required that will take up large memory space and require complex interpolation implementation. In light of these drawbacks, an online calculation approach is adopted where the T_{sw} and $T_{d,a}$ are calculated in real-time. To facilitate simplified calculations, linear approximations can be utilized to curve-fit (6) and the calculation of $C_{eq,Q}$ as functions of V_C. Furthermore, an increased margin ΔI_0 can be added to $I_{0,min}$, to move slightly away from the ZVS borderline. As a result of the aforementioned considerations, provided dead-times will be slightly larger than required, and the current ripple will be slightly larger than the achievable minimum. As such the losses in the circuit will slightly increase; as a point of reference, the predicted CEC efficiency drop for design point R2 assuming ΔI_0 = 0.5 A with linearized online calculation is increased from 1.008% to 1.101%. With the near-negligible increase in circuit efficiency drop, three-dimensional LUTs and corresponding challenges are eliminated, as all calculations can be performed online.

C. Controller Design

The closed-loop system in Fig. 8(a) and Fig. 8(c) need to be analyzed in order to design proper LPF and PI compensators for the average current control loop.

As a non-linear time-varying dynamical system, the plant transfer function varies with V_C and $i_{L,avg}$ operating points. The approach of quasi-static approximation discussed in [25] is taken assuming that the DLF variations are much slower than the current control dynamics such that the circuit always operates at a quiescent operating point changing slowly along the DLF cycle. In this case, an equilibrium analysis can be performed to design the average current controller with the time-varying transfer functions and the system loop gain is analyzed at all operating points.

[3]The instantaneous inductor current change during the dead-time after the synchronous device turns off is relatively small and can be neglected, as I_{pk} is typically much larger than the other switching instant currents.



(a) (b)

Fig. 9. Family of bode plots with identified minimum phase margin for the (a) CCM design, and (b) CRM design. The 400 W line cycle is considered with the design specifications from Table II and controller parameters from Table IV. An input capacitance of C_{in} = 100 μF is utilized for both designs.

The plant transfer function describing the perturbation of d to that of i_L for the APD circuit, is derived using the approach in [25] as

$$P(s) = \begin{cases} \dfrac{V_C^3 Cs + 2V_C V_{in} i_{L,avg}}{V_C^2 LCs^2 + V_{in} i_{L,avg} Ls + V_{in}^2}, & i_{L,avg} > 0 \\ \dfrac{V_C V_{in} C_{in} s + V_C \left| i_{L,avg} \right|}{V_{in} LC_{in} s^2 + \left| i_{L,avg} \right| Ls + V_{in}}, & i_{L,avg} < 0 \end{cases} \tag{17}$$

where C_{in} is the input capacitance, V_{in}, V_C, and $i_{L,avg}$ describe DC-DC operating points which is time-varying across the DLF period.

A PI controller is used as the error-driven compensator for simplicity. The compensator transfer function, described by the gain G_{PI} and corner frequency $f_{c,PI}$, can be written as

$$C(s) = G_{PI}\left(1 + \frac{2\pi f_{c,PI}}{s}\right). \tag{18}$$

The system loop gain can hence be written as

$$H_{loop}(s) = P(s)L(s)C(s) \tag{19}$$

where $L(s)$ defines the transfer function of the LPF. By analyzing $H_{loop}(s)$, the LPF and PI controller parameters can be designed considering desired attenuation of switching ripple, low-frequency gain, crossover frequency, and phase margin. Both low frequency and high frequency properties need to be considered in the system-level controller design, where the low frequency (120 Hz) gain of the system determines the average current tracking performance, and the high frequency properties affect the system stability.

In comparison to CCM designs that typically utilize a larger value of inductance for reduced current ripple, smaller inductances are utilized in CRM. All else the same, this reduction in inductance has two impacts on system design. First, the inductor current has increased current ripple ($>= I_{L,avg}$ at all operating points) and the minimum switching frequency may be less than the nominal frequency in CCM. In addition, the inductor current ripple is maximized when the switching frequency is at the minimal value. In light of this, a high-attenuation low-pass filter is required, often necessitating at least a second-order design with a corner frequency at most one decade below the minimum switching frequency. In contrast, a first-order low-pass filter is more than sufficient in most CCM designs. The second design difference in CRM is that the high-frequency pole is larger due to the smaller inductance value (cf. (17)). Therefore, the high frequency gain of the plant in CRM is inherently increased, requiring a PI controller with less gain to achieve a similar crossover frequency. With this in mind, it can be extended that the low-frequency gain of the compensated CRM system will also be lower than CCM, which could result in inferior current tracking.

TABLE IV
SYSTEM PARAMETERS AND PROPERTIES FOR CCM AND CRM DESIGNS

Controller Parameter		CCM	CRM
LPF	Type	1st order	2nd order (Butterworth)
	Corner frequency	50 kHz	25 kHz
PI Controller	Gain	0.02	0.004
	Corner frequency	2.5 kHz	4 kHz
Loop properties	Max. f_{cr}	18.9 kHz	10.4 kHz
	Min. PM	60°	30°

The LPF and PI controller have been designed independently for the CCM and CRM systems from Table II through a heuristic approach. The following three critical targets were considered: 1) maximum current ripple after the analog LPF less than 0.5 A (when translated from the sensed domain to the true current domain), 2) the system crossover frequency should be around a decade below the switching frequency, and 3) the minimum phase margin greater than 30°. It must be considered for the APD controller design that the DC-DC design point is constantly varying. Nevertheless, there will always exist one operating point for a particular system design in which the phase margin is the minimum, and the cross-over frequency (f_{cr}) is the maximum; this is to say that a system design that achieves stability at this operating point ensures stability at all other operating points. The loop transfer function bode plots for the family of DC-DC operating points at the 400 W average power level for the CCM and CRM systems are shown in Fig. 9, with the system parameters in Table IV. It is clear that each of the three system targets are met in both the CCM and CRM designs, though the minimum phase margin is roughly 30° higher in CCM.

As previously described, an inherent disadvantage of the system design for CRM is lower 120 Hz gain. In order to improve the low-frequency tracking ability in CRM, an improved control solution is proposed in Fig. 10, where a feed-forward term d_{ff} is added to the closed-loop controller duty cycle output. This feed-forward term can be calculated easily by dividing the predicted low-side switch on-time $T_{ls,on}$ by switching period via

$$d_{ff} = \frac{T_{ls,on}}{T_{sw}} = \begin{cases} (I_{pk} - I_0)/(V_{in} T_{sw}), & i_{L,avg} > 0 \\ \left| I_{pk} - I_{on} \right| / (V_{in} T_{sw}), & i_{L,avg} < 0 \end{cases} \tag{20}$$

With the sum of feed-forward prediction and closed-loop compensation, the output of PI controller will only compensate for the remaining error with the use of d_{ff}, such that lower

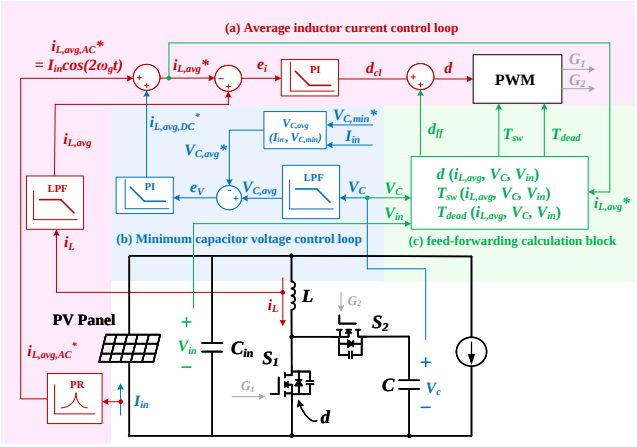


Fig. 10. Illustration of the proposed control strategy of CRM APD and top-level block diagram of the test setup.

gain PI controller is required. The full CCM and CRM control structures with dual control loops and a few predictive calculation blocks are shown in Fig. 10.

1) Average inductor current loop: The current controller serves as an inner loop controlling the average inductor current to track the provided reference, which contains a sinusoidal AC component (DLF component of the main-circuit inverter current, can be drivied from the sensed input current I_{in} passing through a proportional-resonant filter with high gain) and a DC component (derived from the outer average voltage control loop). The sensed inductor current is first passed through an analog LPF to attenuate the switching frequency components in the inductor current, returning only the switching-period-average. Next, $i_{L,avg}$ is compared to the current reference, where the error is controlled to zero with a PI controller. The output of the PI controller will work as a closed-loop term of the S_1 duty ratio, d_{cl}, adding to an optional feed-forward predicted duty ratio, d_{ff}. The S_1 duty ratio d is finally converted to the gate drive signal of the two switches by a PWM block, where the pulse-width is modulated by comparing d to a switching frequency carrier waveform.

2) Feed-forwarding calculation block: As explained in the previous paragraphs, an additional feed-forward dynamic calculation block is utilized in tandem with the current controller in CRM. The duty ratio of the switch pairs will be generated from the sum of the feed-forward dynamically calculated duty ratio and a closed-loop term from the average inductor current tracking PI controller. In addition, variable switching period and dead-time are provided by online calculation blocks according to the sensed input voltage, capacitor voltage, and the reference average inductor current, such that ZVS of both switches can be achieved.

3) Minimum capacitor voltage loop: A low bandwidth outer-loop PI controller is used to control the average APD capacitor voltage to a desired value. Due to the fact that the outer capacitor voltage controller can be the same in both CCM and CRM, specific design details are not discussed for brevity. Generally, the sensed APD capacitor voltage is passed through a LPF with a low cut-off frequency to extract its DLF-

TABLE V
REQUIRED VARIABLES IN PROPOSED CONTROL STRATEGY OF CRM APD
LOCATIONS REFER TO DIFFERENT FUNCTIONAL BLOCKS IN FIG. 10

Location	Variable	Source
(a)	Inductor current i_L	Current sensor (Hall IC ACS730)
(b), (c)	Capacitor voltage V_C	Voltage sensor (Resistive divider)
(c)	Input voltage V_{in}	Voltage sensor (Resistive divider)
(a), (b), (c)	Input current I_{in}	Current sensor (Hall IC ACS722)
(b)	Minimum capacitor voltage $V_{C,min}$	Pre-determined in design stage, selected as 5 V above V_{in}

average $V_{C,avg}$. Next, $V_{C,avg}$ is compared to a determined voltage reference, and the error is controller to zero with a PI controller. The output of the PI controller will work as the DC component of the inner loop average inductor current reference $i^*_{L,avg,DC}$ to compensate for the energy loss in APD to keep the capacitor voltage range unchanged. Another look-up-table or dynamic calculation block can be added in the outer loop voltage controller to determine the average capacitor voltage reference $V^*_{C,avg}$ from the desired minimum capacitor voltage $V^*_{C,min}$ and input current (representing the input power level of the PV panel). With the $V_{C,avg}$ block, fixed $V_{C,min}$ is controlled for the APD at different power level to avoid unnecessary loss caused by the high voltage offset under lower power condition with lower voltage swing.

All variables required and their determination in Fig. 10 are summarized in Table V. It is important to note that the proposed control architecture does not introduce any additional sensor compared to CCM. With the dual-loop control structure and predictive calculations, a simple control strategy without ZCD can be realized for CRM-based APD circuits. The presented flowchart in Fig. 10 also applies to CCM with only the average inductor current control loop and minimum capacitor voltage control loop active.

V. EXPERIMENTAL VERIFICATION

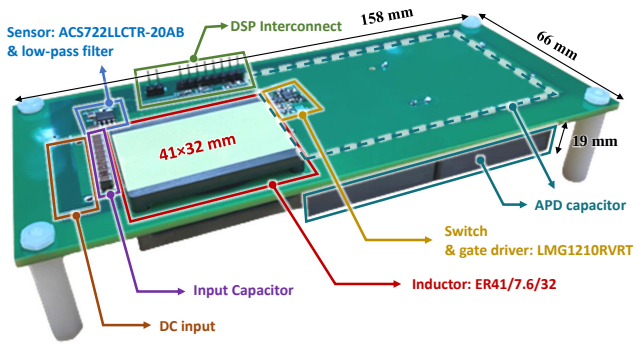
A. Experimental hardware

Two hardware prototypes with near-optimal CCM and CRM design specifications for the APD circuit in a 40 V, 400 W microinverter were built as shown in Fig. 11. To isolate the performance of the APD, standalone PCBs were designed for the CCM and CRM prototypes. Components and modulation details for the two designs are specified in Table VI. Testing setup is shown in Fig. 12, with connections and measurements shown in the architecture block diagram of the setup in Fig. 13. The single-phase inverter prototype in [26] is used in the testing. When testing with standalone APD, load resistor is connected directly in parallel with APD, providing bidirectional average inductor current.

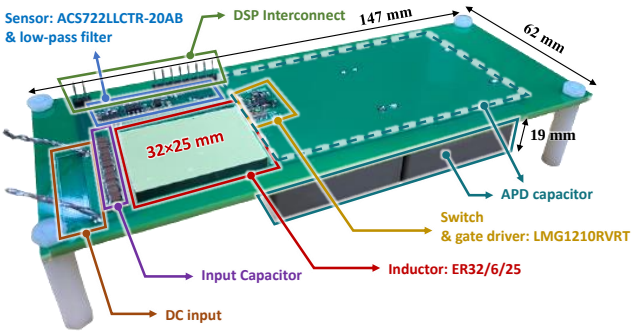
B. Steady-state performance

Experimental verification of the closed-loop operation of the CCM and the CRM design was conducted using the hardware in Fig. 11.

Steady-state closed loop results showing sinusoidal current tracking at the I_{in} = 3 A (120 W) and I_{in} = 7.5 A (300



(a)



(b)

Fig. 11. Annotated photographs of the near-optimal hardware prototypes for (a) CCM, and (b) CRM.

TABLE VI
HARDWARE PROTOTYPE SPECIFICATIONS AND MODULATION PARAMETERS IN EXPERIMENTAL TESTS FOR CCM AND CRM APD.

Design Parameter	CCM	CRM
Switch	200 V GaN devices EPC2207	
Capacitor	132 μF (4 $\times$ 33 μF KEMET R60 film capacitors)	
Inductor Core	ER41/7.6/32-3F36	ER32/6/25-3F36
Air Gap L_g	226 μm	354 μm
Turns N	4	4
Inductance L	22 μH	8.9 μH
Switching Frequency	f_{sw} = 200 kHz	$f_{sw,max}$ = 1 MHz

W) operating points are compared in Fig. 14. Much higher inductor current ripple, where in particular the inductor crosses zero in every switching period, is visible in the CRM test results, representative of the desired high-frequency operating principle for full-ZVS achievement.

Furthermore, zoom-in of the converter steady-state high frequency performance at two example operating points are shown in Fig. 15, In CCM (cf. Fig. 15(a)-(c)), the inductor current ripple is relatively small, where in particular the inductor current does not change direction within a switching cycle. At the asynchronous device transition, the parasitic capacitance of the asynchronous device (S_1 in positive half cycle) cannot be discharged before turning on, and hard switching will occur. At the synchronous device transition, natural ZVS can be achived. In CRM (cf. Fig. 15(d)-(f)) the inductor current ripple is much larger, where the current crosses zero before the synchronous device turns off. In light of this, at the asynchronous device

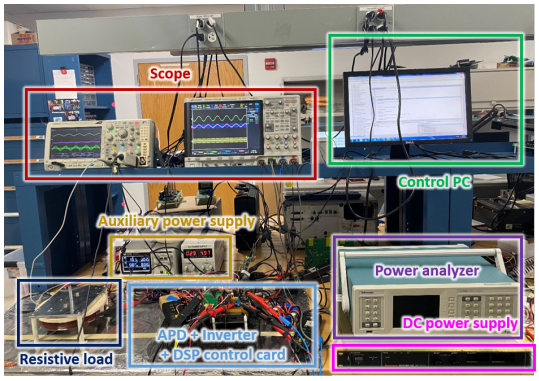


Fig. 12. Testing setup of APD experimental verification

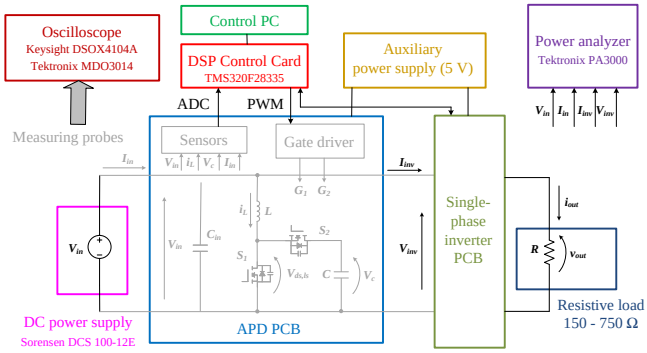


Fig. 13. Architecture block diagram of the testing setup of APD experimental verification

transition, the asynchronous device parasitic capacitance is discharged with sufficient negative inductor current and proper dead time whereby S_1 can be turned on with ZVS with little reverse conduction time. When operating at lower $i_{L,avg}$ near the current zero-crossing, switching frequency will increase to guaruantee the CRM modulation (cf. Fig. 15(g)-(i)).

The thermal performance of the APD circuit at I_{in} = 7.5 A (300 W) is shown for the CCM and CRM prototypes in Fig. 16, with no additional components for thermal management. Thermal measurements were obtained using an infrared thermal imaging camera (FLIR E6), which reveal a thermal hot-spot around the switch-node for both cases with a similar peak temperature of 37.7 °C and 38.9 °C for CCM and CRM, respectively. In CRM, the increased current ripple also leads to increased inductor winding and core losses hence increased inductor temperature, which is consistent with the discussion around Fig. 6.

C. Dynamic performance

Transient tests are conducted to verify the dynamic response of the closed-loop current and average capacitor voltage controllers. To perform this test, a signal generator is utilized to emulate the DLF component of the single-phase inverter DC-side current providing the AC component of the average inductor current reference (cf. Fig. 10).

Step-up and step-down transients tests are analyzed between two input power levels I_{in} = 3 A (120 W, 30% power) and

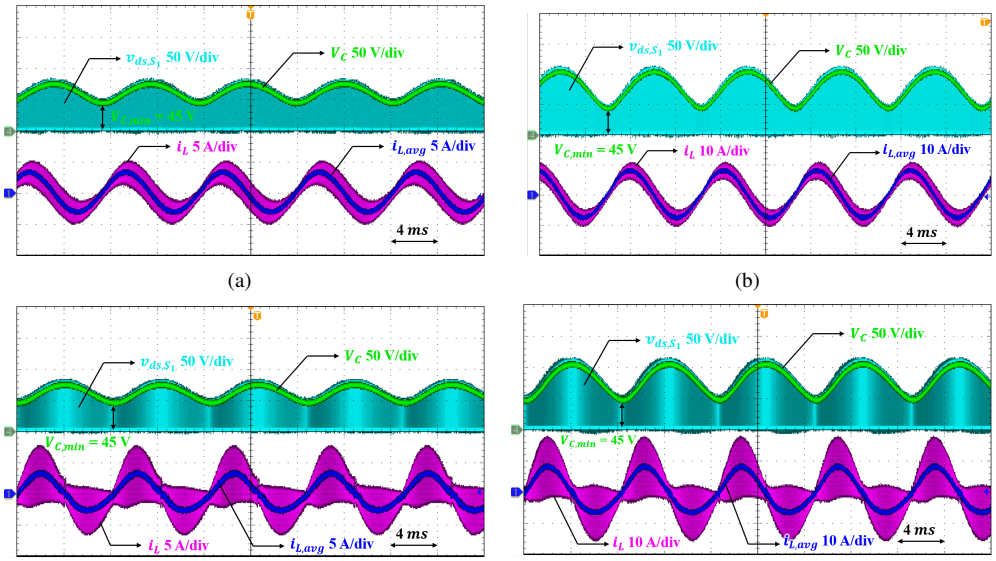


Fig. 14. Experimental steady-state closed-loop results for capacitor voltage (green), low-side switch S_1 drain-source voltage $V_{ds,S1}$ (cyan), low-frequency inductor current (blue), and high-frequency inductor current (purple) in (a) CCM at P_{in} = 120 W, (b) CCM at P_{in} = 300 W, (c) CRM at P_{in} = 120 W, and (d) CRM at P_{in} = 300 W.

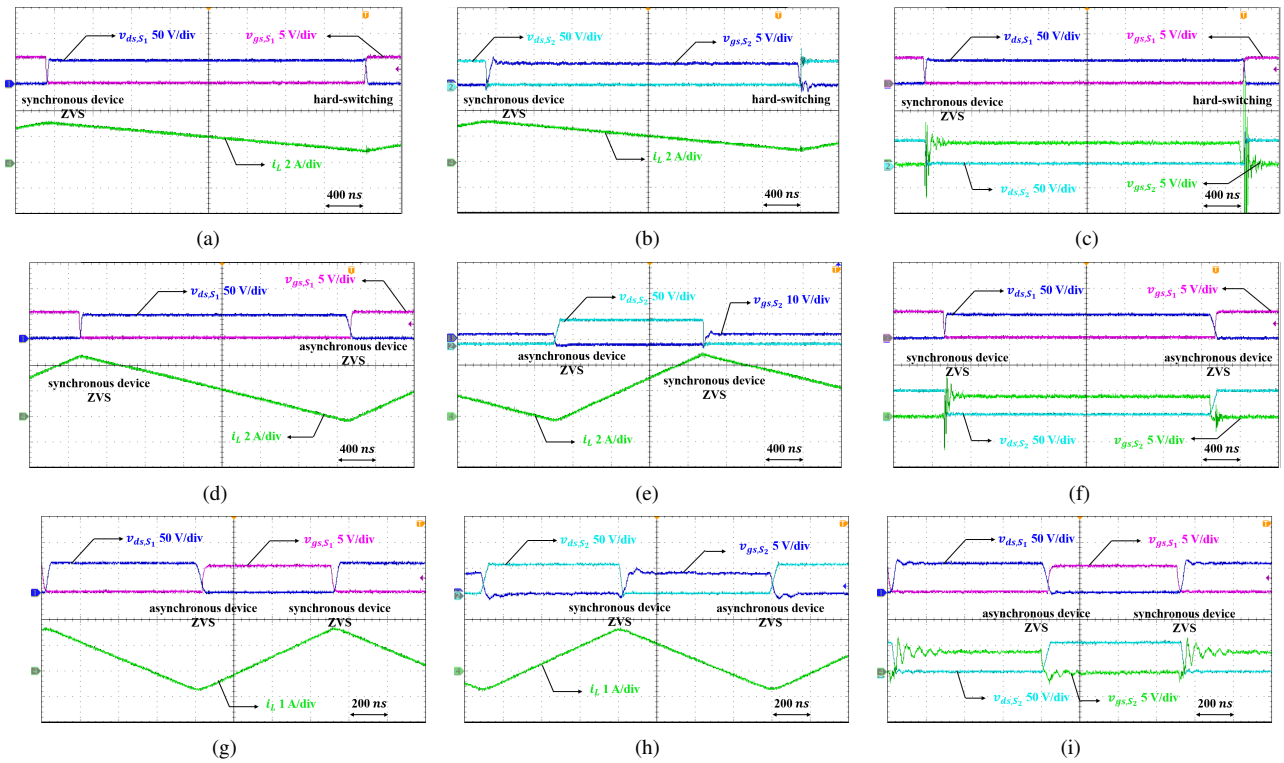
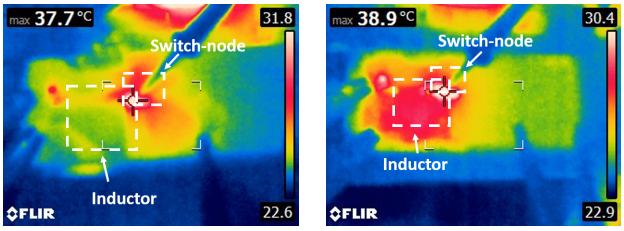


Fig. 15. High frequency waveform of steady-state operation, including (a) CCM APD i_L and S_1 waveform at $i_{L,avg} = 2.5A$, V_C = 50 V, (b) CCM APD i_L and S_2 waveform at $i_{L,avg} = 2.5A$, V_C = 50 V, (c) CCM APD S_1 and S_2 waveform at $i_{L,avg} = 2.5A$, V_C = 50 V, (d) CRM APD i_L and S_1 waveform at $i_{L,avg} = 2.5A$, V_C = 50 V, $f_{sw} = 220kHz$, (e) CRM APD i_L and S_2 waveform at $i_{L,avg} = 2.5A$, V_C = 50 V, $f_{sw} = 220kHz$, (f) CRM APD S_1 and S_2 waveform at $i_{L,avg} = 2.5A$, V_C = 50 V, $f_{sw} = 220kHz$, (g) CRM APD i_L and S_1 waveform at $i_{L,avg} = 0.5A$, V_C = 60 V, $f_{sw} = 580kHz$, (h) CRM APD i_L and S_2 waveform at $i_{L,avg} = 0.5A$, V_C = 60 V, $f_{sw} = 580kHz$, (i) CRM APD S_1 and S_1 waveform at $i_{L,avg} = 0.5A$, V_C = 60 V, $f_{sw} = 580kHz$.



(a) (b)

Fig. 16. Thermal measurements at P_{in} = 300 W for (a) CCM, and (b) CRM, showing higher switch node temperature and lower inductor temperature in CCM, compared to CRM.

I_{in} = 7.5 A (300 W, 75% power) representing the solar irradiance change of PV input. The results of each test for the CCM and CRM prototypes are shown in Fig. 17, where the inductor current tracks the new sinusoidal reference nearly instantaneously due to the high bandwidth of the current controllers. Furthermore, the average capacitor voltage controller settles after 10 to 15 DLF periods, due to significantly lower control loop bandwidth. Importantly, the CRM control loop both tracks the new reference and maintains ZVS performance, regardless of the low-frequency settling time of the capacitor voltage controller, with the considered dynamic calculation block. In light of the demonstrated results, the CCM and CRM prototypes have near-equal performance from a dynamic control perspective, with appropriate design of each of the current control systems.

D. Efficiency

To verify the efficiency performance of the realized near-optimal design, the average power loss of the APD was measured by taking the difference between the average power sourced from the DC supply and the power dissipated in a resistor, connected in parallel to the supply and the APD. The power losses measured using a PA3000 power analyzer were compared to predictions from the utilized loss model, with results up to the 300 W operating point presented in Fig. 18. It is evident that the expected and measured power losses, and hence efficiency drop, agree very closely at all operating points in both CCM and CRM, validating the loss model utilized in the optimization procedure. Based on the measured efficiency at different power points, the experimental CEC efficiency drop for the CCM and CRM prototypes are ∼0.87% and ∼0.99%, respectively, which closely match the theoretical optimal CEC efficiency values in Section III-C.

E. Full-system verification

Experimental verification of the full microinverter system operation of the CCM and CRM APD integrated with single-phase inverter was conducted with the setup shown in Fig. 12 and the connection and measurement shown in Fig. 10 collecting collect the information for both dc-side and ac-side of the single-phase inverter. Resistive load R = 288 Ω is used to emulate the grid side with unity power factor, corresponding to average power of 200 W and output voltage of 240 V RMS voltage.

For single-phase inverter operating at 200 W in steady state, the AC-side waveforms are shown in Fig.19(a), where both output voltage and current are sinusoidal with a frequency of 60 Hz in such that the output power is fluctuating with a frequency of 120 Hz. On the DC-side, use of either the CCM APD, as in Fig. 19(b) or CRM APD, as in Fig. 19(c), is sufficient to control the input current I_{in} to be flat with low ripple content, eliminating the fluctuation of DC-side power.

Testing with quasi-PV source consisting of a DC voltage source and a resistor in series [10], [17] was conducted to evaluate the performance of APD in the single-phase inverter system with a source featuring a similar output characteristic as PV panel. Voltage source V_s = 20 V and resistor R = 8 Ω are used for the quasi-PV source testing with a maximum power at the voltage V_{mp} = 10 V and current I_{mp} = 1.25 A. In the testing implementation, the single-phase inverter operating point moves along the I-V curve of the quasi-PV source by changing the input voltage reference from the effective open-circuit voltage, V_{OC} (which is equal to the DC source voltage V_s), to V_{mp} in 1 V increments. This emulates the commonly-used perturb and observe maximum power point tracking (MPPT) algorithm. The APD action is evaluated by measuring the quasi-PV source voltage and current (i.e. between the series resistor and the converter), of which the DLF components are removed through control of the input current (cf. Fig. 10). Experimental testing results are presented in Fig. 20(a) and (c), which demonstrate stable and adequately fast transient response of the APD circuit following each step change of operating point. The steady-state performance of input DLF rejection can be observed from the zoom-in waveform in Fig. 20(b), where the voltage and current ripple of the quasi-PV source are attenuated by the APD. Furthermore, as shown by the zoom-in at one of the step change instants in Fig. 20(d), the settling time after each step perturbation is less than 10 ms. With main-circuit input perturbations separated by about 2 s (much greater than the settling time of the APD), satisfactory APD operation along with emulated MPPT is achieved.

VI. Conclusion

This manuscript has presented a comprehensive comparison between CCM- and CRM-based parallel boost APD for microinverter applications from the broad perspectives of multi-objective design and controller implementation. The key contributions and conclusions are as follows: 1) development of a multi-objective design framework enabling minimization of three objectives (CEC efficiency drop, system volume, and system cost) for CCM and CRM, considering a decision space encompassing the GaN-based device selection, inductor design, capacitor bank design, and switching frequency. 2) Results of the multi-objective design optimization demonstrated that the selected designs in CCM and CRM exhibit near-equal CEC efficiency drop (0.82% for CCM and 0.88% for CRM), while CRM enables reduction in both system volume (2% reduction) and system cost (3.8% reduction) due to the lower inductance requirement facilitating the use of a smaller inductor core (ER32 in CRM versus ER41 in

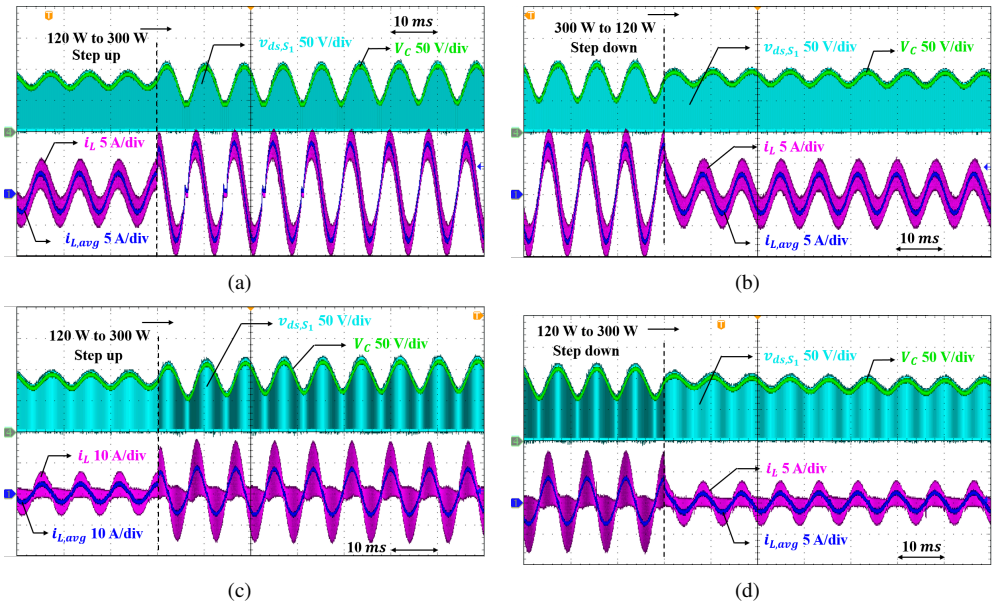


Fig. 17. Experimental closed-loop results of transient testing for capacitor voltage (green), low-side switch S_1 drain-source voltage $V_{ds,S1}$ (cyan), low-frequency inductor current (blue), and high-frequency inductor current (purple) in (a) CCM from P_{in} = 120 W to P_{in} = 300 W, (b) CCM from P_{in} = 300 W to P_{in} = 120 W, (c) CRM from P_{in} = 120 W to P_{in} = 300 W, and (d) CRM from P_{in} = 300 W to P_{in} = 120 W.

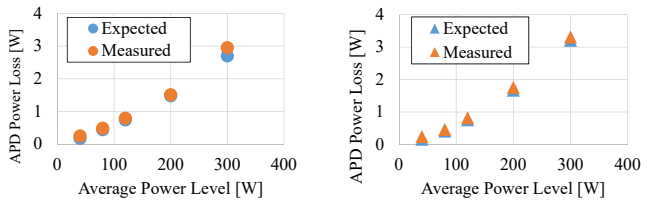


Fig. 18. Comparison between measured and loss model predicted APD power loss at different power levels for (a) CCM, and (b) CRM. At lower power levels, CCM shows similar power loss to CRM but it slightly outperforms CRM at higher powers, due to the higher conduction losses in CRM.

CCM). 3) A novel PI-based closed-loop control architecture is proposed for CRM operation, which unlike conventional CRM implementations does not need an accurate ZCD module while also realizing ZVS of both APD devices through accurate dynamic online calculations. 4) The closed-loop control analysis concluded that both systems can achieve satisfactory closed-loop performance, though the low-frequency gain and phase margin in CRM is generally lower than that of the CCM design, and the CRM implementation is increased in computational complexity as dynamic calculations are utilized. Experimental implementation of the CCM and CRM closed-loop controllers confirmed the steady-state and dynamic performance, validating the controller design analyses and the proposed CRM control implementation. Future work will explore the feasibility of other APD architectures in the same application.

APPENDIX

A. Loss Model in Design Optimization

1) Operation Analysis: In order to accurately predict the CEC efficiency drop of APD for a considered design set, low- and high-frequency operation analysis should be conducted. When operating at a given power level, low frequency inductor current profile for a DLF period is described by (1), and the capacitance value (base capacitor multiplied by the number in parallel) in the design set and selected $V_{C,min}$ are used to determine the trajectory of the APD capacitor voltage via (2). While the switching frequency and inductance are used to determine the switching period profile of the high-frequency inductor current, of which the peak-to-peak current ripple in CCM is calculated across the line-cycle according to,

$$\Delta I_{pp}(t) = \frac{V_{in}(V_C - V_{in})}{V_C L f_{sw}}, \tag{21}$$

and in CRM according to,

$$\Delta I_{pp}(t) = I_{pk}(t) - I_{valley} = 2i_{L,avg}(t) - I_{valley}, \tag{22}$$

where I_{pk} is peak current and I_{valley} is valley current in a switching period as defined in Fig. 3. The estimation of I_{pk} and I_{valley} is introduced in Section IV-B.

The RMS current across the line-cycle can hence be calculated assuming triangular wave via,

$$I^2_{L,rms}(t) = I^2_{L,avg}(t) + \frac{1}{12}\Delta I^2_{pp}(t). \tag{23}$$

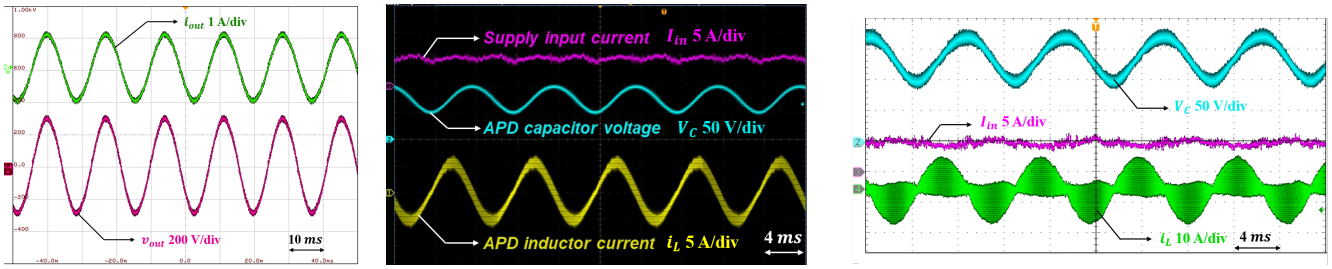
With this information, all of the losses in the circuit can be determined via the detailed loss model discussed below.

2) Device Loss: Device conduction loss is calculated by,

$$P_{sw,cond} = R_{ds,on} I^2_{L,rms}, \tag{24}$$

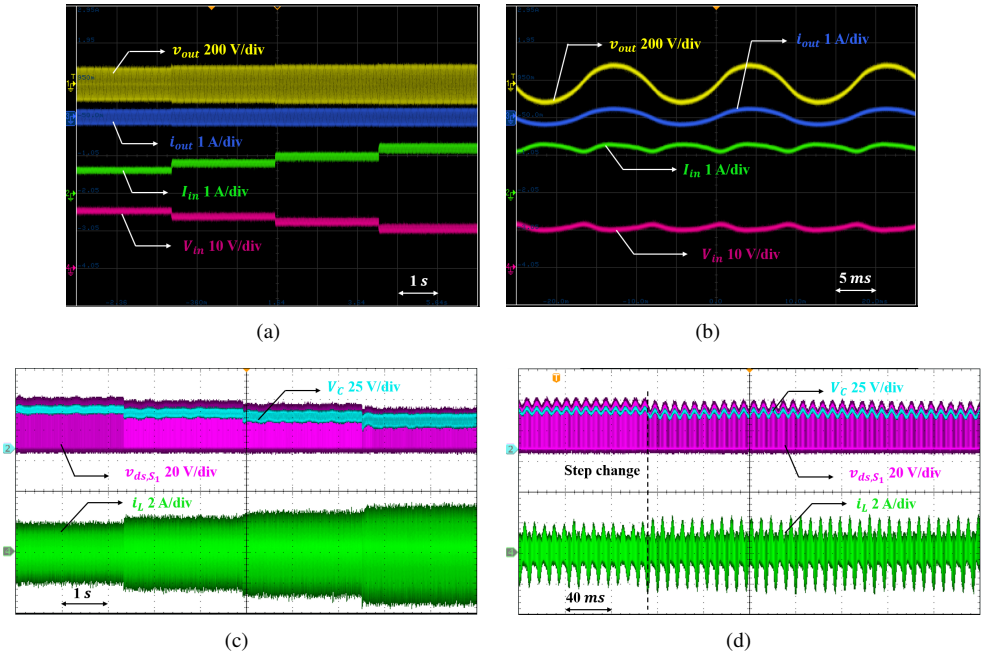
where $R_{ds,on}$ is the device on-state resistance and $I_{L,rms}$ is the inductor RMS current.

Device switching loss is only considered for one hard switching device in CCM and is treated negligible when ZVS



(a) (b) (c)

Fig. 19. Experimental closed-loop results for full system verification involving integrated operation of the APD and the inverter main ciruit. (a) AC-side voltage v_o and current i_o at steady state P_{in} = 120 W, (b) DC-side input current I_{in}, APD capacitor voltage V_C, inductor current i_L for CCM at steady state P_{in} = 120 W, and (c) DC-side input current I_{in}, APD capacitor voltage V_C, inductor current i_L for CRM at steady state P_{in} = 120 W.



(a) (b) (c) (d)

Fig. 20. Experimental closed-loop results for full system verification using quasi-PV source with 20 V voltage source and 8 Ω resistor, involving integrated operation of the APD and the inverter main circuit, (a) DC-side voltage V_{in}, DC-side current I_{in}, AC-side voltage v_o and current i_o under step changes from $V_{in} = 14V$ to $V_{in} = 10V$, (b) zooming-in of DC-side voltage V_{in}, DC-side current I_{in}, AC-side voltage v_o and current i_o at steady state maximum power point $V_{mp} = 10V$, $I_{mp} = 1.25A$, (c) CRM APD capacitor voltage V_C, inductor current i_L under step changes from $V_{in} = 14V$ to $V_{in} = 10V$, and (d) zooming-in of CRM APD capacitor voltage V_C, inductor current i_L under steps changes from $V_{in} = 14V$ to $V_{in} = 13V$.

is achieved. The approach introduced in [27] is utilized, which considers detailed switching transition modeling including the effects of parasitic inductance, capacitance, and gate resistance. The considered parasitic parameters can be found in [1]. Turn on switching loss is calculated by,

$$P_{sw,on} = \frac{1}{2}\left[t_{ri}I_0 + \frac{1}{2}t_{fv}(I_0 + 2I_{oss})\right](V_C - V_{Ld})f_{sw} \quad (25)$$

$$V_{Ld} = L_d(I_0 + 2I_{oss})/t_{ri} \quad (26)$$

$$t_{ri} = -\ln(1 - \frac{I_x}{g_m(V_g - V_{th})})(C_{gs}R_g + L_s g_m) \quad (27)$$

$$t_{fv} = Q_{oss}/I_{oss} \quad (28)$$

where I_0 is the inductor current value at the turn off instant of synchronous device (starting instant of hard-switching), L_s and L_d are parasitic source and drain inductances, V_{Ld} is the voltage drop due to drain inductance, V_g is the gate turn on voltage, V_{th} is the gate threshold voltage, R_g is the gate resistance, and g_m is the transconductance, which can be modeled by

$$g_m = \left[\frac{k_1(I_x + 2I_{oss})^x}{(I_x - I_{oss} - k_2)}\right]^{\frac{1}{x}}, \quad (29)$$

where k_1, k_2, and x are coefficients extracted from curve-fitting the $i_d \sim v_{gs}$ curve by $i_d = k_1(v_{gs} - V_{th})^x + k_2$. Further, I_{oss} is the current required to recharge the parasitic capacitances at turn on transitions, given by

$$\frac{2L_s}{Q_{oss}}I_{oss}^2 - \left(\frac{2}{g_m R_g} + \frac{C_{gd}}{C_{gd}+C_{ds}}\right) I_{oss} + \frac{1}{R_g}(V_g - V_{th} - \frac{I_0}{g_m}) = 0, \quad (30)$$

where C_{gs}, C_{ds} and C_{gd} are voltage dependent parasitic capacitance and the corresponding linearized charge equivalent value can be taken. Reverse recovery loss is not considered for eGaN device due to zero reverse recovery charges [28]. Turn-off loss is treated negligible for the ultra-fast turn off GaN device.

Reverse conduction loss (i.e. 3rd quadrant device conduction) is an additional loss mechanism during the device dead-time, can be calculated by

$$P_{sw,rev} = [I_{pk}(T_{d,s} - t_{zvs,s}) + I_0(T_{d,a} - t_{tr})]V_F f_{sw} \quad (31)$$

where V_F is the forward conduction voltage, $t_{ZVS,s}$ is minimum dead time required for the soft-switching device to facilitate the ZVS transition according to [21], and $t_{tr} = t_{ri} + t_{fv}$ is the hard-switching transition time. Modulator provided dead time as defined in Fig. 4 are selected as fixed 33 ns for both devices in CCM and only $T_{d,s}$ in CRM. The second term in (31) is neglected for the asynchronous device in CRM assuming $T_{d,a}$ controlled to be close to the ZVS time in (6).

3) Inductor Loss: Inductor core loss is calculated using the General Steinmetz Equation,

$$P_{L,core} = \frac{V_e}{T_{sw}} \int_0^{T_{sw}} k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B_{pp})^{(\beta-\alpha)} dt \quad (32)$$

where K_i, α, and β can be derived from the Steinmetz parameters of the core material, ΔB_{pp} is the peak-to-peak flux density in the core in the switching period, and V_e is the effective volume of the core [29].

Winding loss is calculated by

$$P_{L,cond} = R_{L,dc} I_{L,rms}^2 + \sum_f R_{L,ac(f)} I_{L(f)}^2 \quad (33)$$

considering both the DC resistance, and frequency-dependent AC resistance at multiple frequency components of i_L.

4) Capacitor Loss: Capacitor ESR loss is calculated with,

$$P_{C,esr} = \sum_f ESR_{(f)} I_{C(f)}^2 \quad (34)$$

considering four low-frequency (DLF) harmonics of the switching period averaged capacitor current I_C added.

B. Component database in Decision Space

1) Device database: The considered GaN-based devices in the decision space are listed in Table VII. It is clear that a variety of devices are considered with unique rated voltages and currents, and associated device parameters such as drain-source resistance, output capacitance, and cost.

TABLE VII
DECISION SPACE OF CONSIDERED GAN DEVICES

Device	Voltage Rating [V]	Current Rating [A]	C_{oss} [pF]	$R_{ds,on}$ [$m\Omega$]	Cost [$]
EPC2033	150	48	480	7	4.68
EPC2059	170	24	267	6.8	1.78
EPC2207	200	14	130	22	1.67
EPC2010C	200	22	240	25	3.39
EPC2215	200	32	390	8	3.16
EPC2034C	200	48	641	8	4.31

TABLE VIII
DECISION SPACE OF CONSIDERED FILM CAPACITORS

Capacitance [μF]	Length [mm]	Width [mm]	Height [mm]	Cost [$]
6.8	32	13	12	0.94
10	32	9	17	1.45
15	32	11	20	2.20
22	32	13	22	2.77
	41.5	11	22	
	32	24	15	
33	41.5	24	15	2.99
	41.5	13	24	
	32	14	28	
47	41.5	24	19	5.45
	32	18	33	
	41.5	16	28.5	
68	41.5	19	32	6.33

2) Capacitor database: The considered KEMET R60 series film capacitors with 160 V DC voltage rating in the decision space are listed in Table VIII. It is evident that multiple capacitors with different capacitance, dimensions, and cost, are considered in the base capacitor database.

3) Inductor database: The considered planar ER-core-based inductor designs in the decision space are listed in Table IX. Different number of turns and air gap length are designed to achieve unique inductance values for cores of different size and cost.

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ABRIDGED LEGAL DISCLAIMER

The views expressed herein do not necessarily represent the views of the U.S. DOE or the U.S. Government.

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TABLE IX
DECISION SPACE OF CONSIDERED PLANAR ER CORE BASED INDUCTOR DESIGNS

Core	Modulation	# of turns N	Air gap length [μm]	Inductance [μH] (Simulated)
ER18/3/10	CRM	5	432	3.0
18×9.7 mm		7	620	4.4
$ 2.355		9	768	6.4
ER23/3.6/13	CRM	4	338	3.7
23.2×12.5 mm		7	618	7.0
$ 2.051		10	890	10.9
ER32/6/25	CCM	8	460	31.7
32.1×25.4 mm		10	590	40.5
$ 2.414		11	536	52.9
		14	696	68.3
	CRM	4	354	9.8
		5	444	13.0
ER41/7.6/32	CCM	4	226	22.4
40.6×32 mm		6	340	36.9
$ 3.12		7	346	48.4
		9	458	63.4
	CRM	4	452	12.8
ER51/10/38	CCM	4	236	31.1
51×38.1 mm		5	246	48.9
$ 6.70		6	290	62.3
		7	334	75.2
		8	378	89.1

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