Characterization of a Bare-die SiC-based, Wirebond-less, Integrated Half-bridge with Multi-functional Bus-Bars

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***Abstract*—This article presents detailed analysis and characterization results of a bare-die Silicon Carbide (SiC) MOSFET-based, half-bridge switch module with integrated decoupling capacitors and gate-driver circuitry, suitable for high-performance power electronics in applications like next-generation automotive systems. The module structure enables wirebond-less integration in an entirely PCB-based assembly, featuring compact vertical power and gate loops with low parasitic inductances and capacitances. The assembly uses thermo-electrically multi-functional components, which simultaneously serve as bus-bars and heat sinks, thereby obviating the need for thermal interface material and also allows quasi-double-sided cooling. The paper starts with a comprehensive review of integrated power modules, followed by a description of the module structure under consideration and its various practical design aspects. Thereafter, a detailed discussion is presented on electrical parasitic modeling, conducted using 3D finite element analysis simulations in Ansys Q3D. Results indicate that the module can achieve extremely low values of loop inductances ($L_{loop,power}$ = 1.35 nH, $L_{loop,gate}$ = 5.1 nH at an oscillation frequency of 100 MHz) without entailing high parasitic capacitances, which can provide enhancements in switching performance compared with state-of-the-art solutions. Experiments performed on a proof-of-concept half-bridge prototype, operated upto 600 V, 30 A demonstrate close adherence of the measured electrical parameters with theoretical predictions and acceptable preliminary thermal performance.**

***Index Terms*—Bare-die, SiC, 3D packaging, wire-bond-less, power loop inductance, FEA, double-sided cooling.**

I. Introduction

With the ongoing efforts for wide-scale adoption of electric vehicles (EVs), there has been an ever-increasing demand for high-performance power electronics for various EV subsystems like traction inverters, chargers and auxiliary power converters [1], [2]. Towards this end, the U.S Department of Energy has outlined challenging technical goals for next-generation automotive power electronics, as highlighted by the 2025 targets of exceeding 100 kW/L power-density and 97% efficiency for traction inverters [3]. Improvements in the electrical switching performance, losses and thermal management of semiconductor power devices have been identified as key enabling pathways to achieve these targets [3]. Emerging wide-bandgap (WBG) devices like Silicon Carbide (SiC) MOSFETs offer several advantages in this regard, when compared to Silicon devices used in conventional designs [4]. However, state-of-the-art approaches for power device packaging have fundamental electrical and thermal limitations, which make it difficult to realize the full capability of SiC switches. Conventional half-bridge switch modules [5] employ bare-die devices, typically attached to a direct-bonded-copper (DBC) substrate using wirebonds, as shown in Fig. 1. Such a configuration results in appreciable power and gate loop inductances as the decoupling capacitors and gate-drive ICs are remotely located outside the module. For instance, the half-bridge power module described in [6] has a minimum power loop inductance ($L_{loop,power}$) of 21 nH. This leads to voltage ringing under fast commutation, generates unacceptable switching losses at high switching frequencies and can also lead to spurious gate-drive operation. Moreover, conventional power modules are single-side-cooled, wherein heat is extracted through layers of DBC substrate, baseplate and thermal interface material (TIM), which limits thermal performance.

To address the electrical challenges associated with conventional packaging, researchers have explored several approaches for integration of bare-die SiC devices with decoupling capacitors and/or gate driver ICs in a single compact package, resulting in substantial reduction of parasitic inductances. A broad classification of these approaches is outlined in Fig. 2. A half-bridge switch module with integrated decoupling capacitor using AlN DBC is presented in [7]. The works in [8] and [9] achieve further integration by including the gate driver ICs into the same substrate. A hybrid DBC-PCB approach is proposed in [10], with the power and gate circuit connections formed through an AlN DBC and printed circuit board (PCB) respectively, which allows more design freedom for optimizing the layout of the gate-driver circuitry. While the aforementioned approaches overcome some of the limitations of conventional packaging, they use wire bonds in the assembly which adds inductance, lowers surge current capacity and also poses reliability concerns [11]. In addition, the use of wire bonding precludes the possibility of double-sided cooling (DSC) [12]. To address these concerns, researchers have proposed several wire bond-less integration approaches, some of which are discussed next.

Half-bridge structures proposed in [13] and [14] use AlN and Al_2O_3 DBC substrates respectively and successfully reduce power loop inductance primarily through the use of short and wide planar copper bonds for interconnection between the

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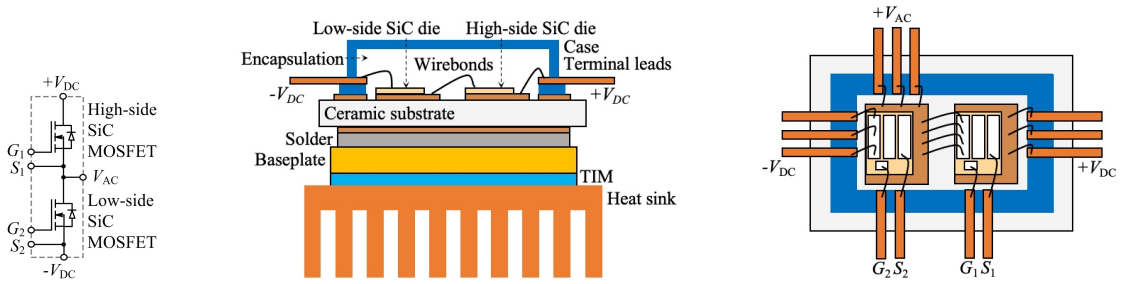


Fig. 1: A conventional wire-bonded power module structure [5]. (a) Schematic. (b) Front view. (c) Top view.

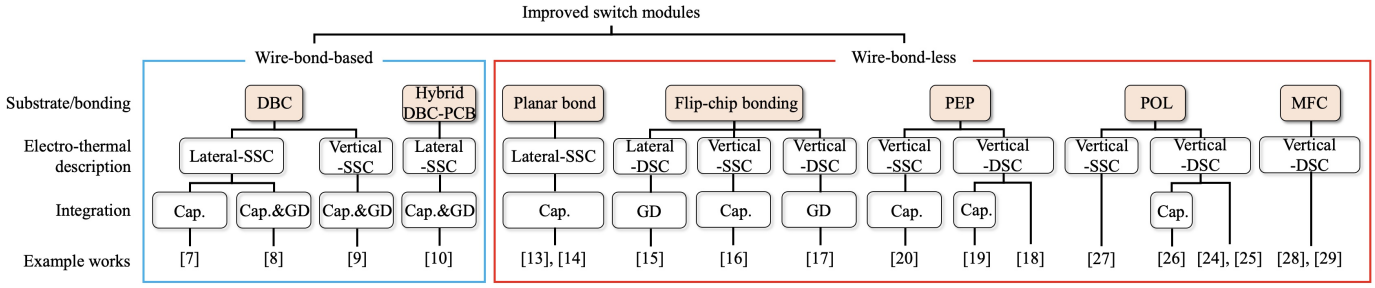


Fig. 2: Overview and classification of recently proposed power module structures. The acronyms DBC, PEP, POL, MFC, SSC, DSC and GD stand for direct bonded copper, PCB-embedded packaging, power overlay, multi-functional component, single-sided cooling, double-sided cooling and gate-driver respectively.

dies. As a result, the designs achieve $L_{loop,power}$ values of 4.5 nH [13] and 1.6 nH [14], respectively. The work in [14] comes close to the minimum loop inductance that lateral designs can achieve, while additionally integrating damping networks, which helps to further mitigate voltage oscillations. However, these structures still entail single-sided cooling involving TIM and substrates, and thus the thermal performance of these configurations is not maximized.

The fundamental approach adopted in [15], [16] and [17] for achieving wire bond-less integration involves flip-chip bonding, whereby the gate and source terminations of the bare-die are directly attached to the substrate. The design in [15] sandwiches the dies between two PCBs or ceramic substrates. Specialized die-attachments are used in [16] to effectively convert the vertical bare-die device to a lateral device and achieve an $L_{loop,power}$ value of 4.88 nH. A concern with these approaches is their thermal management, as they are either single-side-cooled [16] or quasi-double-side-cooled [15], [17].

PCB-embedded packaging (PEP) [18]–[20] represents another approach towards elimination of wire bonds and realization of extremely low power loop inductance. In this method, dies are embedded in a multi-layer PCB, and the power commutation path is formed vertically through the PCB itself. Using the PEP approach, the design in [18] achieved an interconnection stray inductance of 2.09 nH, while [19] and [20] obtained total loop inductance of 2 nH and 0.86 nH respectively. Though PEP is a promising technology, it can be complex and costly due to requirement of specialized facilities for embedding dies into PCBs with elaborate inner blind vias [21]. Furthermore, it requires careful considerations of high electric field stress [22] and thermo-mechanical stress-induced reliability concerns [21], [23].

Another type of wire bond-less power module design involves the use of planar power overlays (POL) for interconnection. In such approaches, the bare dies are located between wide bus-planes, placed close to each other in the z-direction for minimizing power loop inductance. A single-switch module utilizing POL interconnection and wide laminar bus-bars with blade-shaped sockets is presented in [24]. Another approach in [25] uses heat-spreaders as substrates, with the dies directly populated on the heat-spreaders. The work in [26] places switch and diode dies between two DBCs to realize a half-bridge module consisting of a P-cell and an N-cell. In addition to low parasitic inductance, planar POL-based designs can achieve double-sided cooling. The SKiN technology used in some industrial modules [27] involves the use of a flexible PCB-overlay on the top side of the dies to ensure low commutation inductances while maintaining high blocking voltage. As a result, the works in [26] and [27] reported significantly low $L_{loop,power}$ values of 1.63 nH and 1.4 nH respectively. While POL-based designs result in compact, low-inductance modules with DSC, they are likely to result in high parasitic capacitances from the switching node on account of the large overlap area and small distance between the bus-planes. Furthermore, the small distance makes intra-module integration of other components such as capacitors and gate driver circuitry challenging.

The works described in [28] and [29] present a different paradigm towards wire bond-less integration by proposing the use of multi-functional components (MFCs), which act as heat-sinks and electrical bus-bars simultaneously. The heat-sinks are directly attached onto the dies and thus enhance thermal performance by eliminating layers of ceramic substrate and TIM. The power-chip-on-bus (PCoB)-based approach introduced in [28] directly connects both sides of the dies to metal substrates, working as MFCs, thereby achieving enhanced

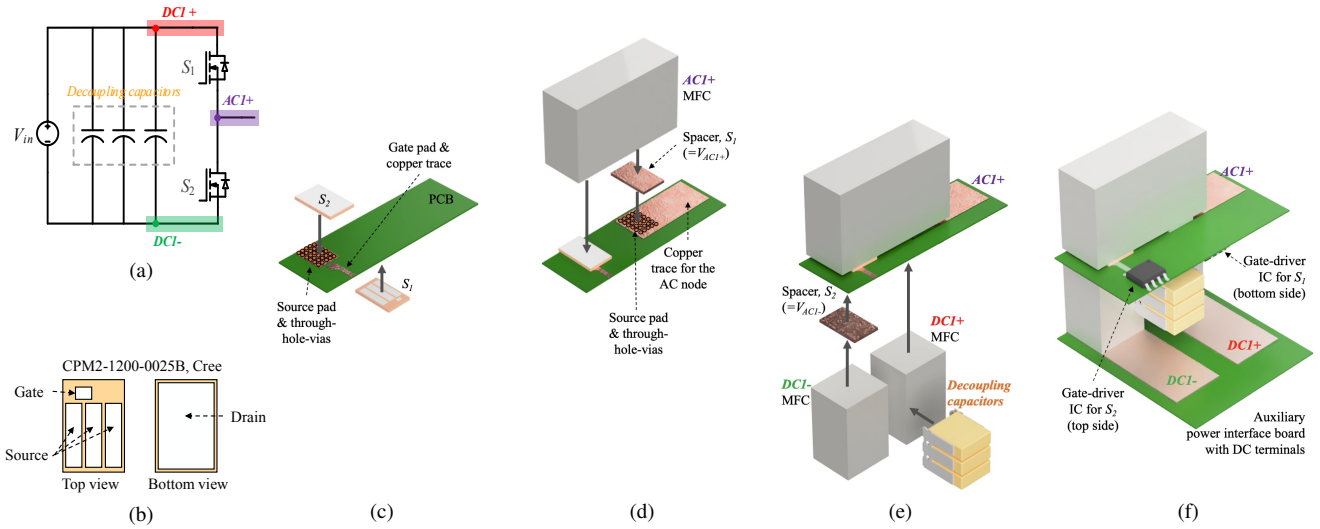


Fig. 3: Conceptual evolution of the switch assembly, whose full-bridge realization was reported in [32]. (a) Schematic of one half-bridge. (b) Selected bare-die SiC MOSFET: CPM2-1200-0025B. (c) Soldering of switches on the PCB. (d) The source of S_1 is connected to the drain of S_2 through THVs, spacer of S_1 and AC1+ MFC. (e) The source of S_2 is connected to DC1- MFC in the same manner through its THVs and spacer of S_2. Decoupling capacitors are attached across the DC MFCs. (f) Final assembly with connections to other components such as transformer and gate driver ICs.

thermal performance with direct DSC. However, close integration of decoupling capacitors and gate driver circuitry might pose a design challenge as this would result in a lesser contact area for the heat sinks. The work in [29] proposed the use of MFCs, with small contact areas between different materials to mitigate thermo-mechanical stress. The main shortcomings of this approach are that it results in high loop inductances since decoupling capacitors and gate-drive circuitry are placed far away from the power path, and it uses wire-bonds to make connections to the gate driver.

In order to address the previously-described shortcomings, a bare-die SiC-based, half-bridge switch module with integrated decoupling capacitors, gate-drive circuitry and heat-sinks was proposed in [30] and [31]. The main advantages of the module structure are i) extremely low parasitic inductances and capacitances, ii) wire bond-less assembly using a PCB substrate and MFCs, iii) good thermal performance due to double-sided cooling through the MFCs and iv) compact layout without sacrificing thermal performance due to the special vertical profile of the MFCs. Basic operational feasibility of the concept was validated in [32] for a 500 kHz, high-power-density, 3.3 kW, dual-active-bridge (DAB) dc-dc converter for the dc-dc stage of on-board charger systems. Satisfactory high-frequency converter performance including improvements in power-density and efficiency were demonstrated in [32], but a detailed characterization of the switch module itself was not attempted. This paper therefore builds on previous work by discussing detailed characterization and practical considerations of the module structure and providing relevant experimental results. In particular, following a description of the module structure, further discussions on diverse aspects like manufacturing, reliability, safety, isolation and EMI are presented in Section II. Extraction of circuit parasitics of interest like inductances and resistances of power and gate loops as well as capacitances using Ansys Q3D simulations is discussed in Section III. The results indicate that the proposed structure can have very low power and gate loop inductances of around 1.5 nH and 5 nH respectively at an oscillation frequency of 100 MHz along with negligibly low values of common-source inductance and parasitic capacitance to the switching node. Moreover, the impact of design variables on the parasitics is investigated to further optimize the design. A comparison with state-of-the-art integrated switch modules is presented in Section IV to highlight the multiple performance improvements realized with the proposed structure. Finally, experimental results demonstrating switching behavior and validating the theoretical modeling are presented in Section V along with some preliminary thermal performance results.

II. PCB-Based Wirebond-less Module with MFCs

A. Description of the Module Configuration

The conceptual development of the wire-bond-less power module structure was explained in detail in [32], albeit for a full-bridge configuration. For the convenience of the reader, steps involved in the evolution of the half-bridge switch module structure are briefly reviewed in this sub-section. As shown in Fig. 3, the structure consists of decoupling capacitors, gate-driver ICs, SiC bare dies and coolers integrated into a single PCB-based package. The approach involves bonding the dies directly to the PCB with the gate and source pads of the die facing the PCB, similar to the flip-chip attachment method in [16]. The high-side and low-side dies are placed on opposite sides of the PCB and interconnection (of the switch node AC1+) between them is done using through-hole-vias, conductive spacers and metallic MFCs. Connections for the dc nodes are realized using similar MFCs, which also hold the decoupling capacitors. As a result of the described arrangement, the power commutation loop is formed vertically through the PCB, as highlighted in Fig. 4.

Furthermore, heat can be extracted from the dies in both directions - directly through the MFC on one side and indirectly through the vias, spacer and MFC on the other. Hence

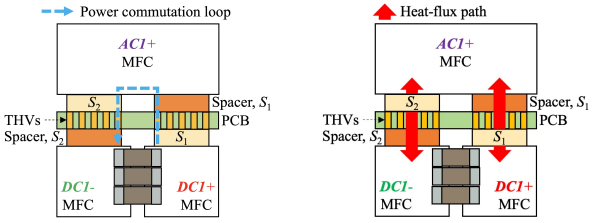


Fig. 4: Front-view of the switch assembly. (a) Power commutation loop. (b) heat-fluxes from the dies.

the cooling of the switches is double-sided, though it may be more accurately described as quasi-DSC, since the vias and spacers lead to greater thermal resistance on the side they are present. While simplest conceptual realization of the MFCs is possible using metal (e.g. copper) blocks or sheets, as depicted by the white blocks in Fig. 3, such an approach based on natural convection is only feasible for low heat-flux applications. For more aggressive thermal management, the cooling performance can be improved through forced-air cooling as in [28] or by using advanced microchannel coolers for the MFCs with dielectric coolant such as 3M Novec [33]. Connection of the module to external dc terminals can be done using an auxiliary interface PCB, as illustrated in Fig. 3f. The interface PCB is placed on the side of the main PCB where the DC MFCs are located. The edges of the DC MFCs are soldered to pads on the auxiliary board and final external connections are made through traces and a dc terminal header.

B. Manufacturing Details and Considerations

An important consideration for implementing the proposed concept is the attachment of the dies onto the PCB. Commercially available bare-die SiC switches are designed for Al wire-bonding of gate and source pads and soldering of the drain pad on DBC. Hence the gate and source pads of commercial dies are metallized with Al, which poses difficulties in soldering [28]. Therefore to enable direct soldering of the gate and source pads of the dies onto the PCB, they were re-metallized. Following an approach similar to [28], this was done by depositing successive layers of titanium, nickel and silver with thickness of 0.3 μm, 0.3 μm and 1 μm respectively in a sputtering unit [34].

As described in section II-A, the module assembly involves stacking different components vertically over small areas on both sides of the PCB. This necessitates the use of multiple solder pastes with different liquidus temperatures (T_{melt}) in a cascade soldering process involving the following sequential steps, which are summarized by the flowchart in Fig. 5.

1) Formation of a solder bump on the gate pad of all dies using high-Pb solder paste (Indium 9.72-HF, T_{melt} >300°C). The bump helps to strengthen and maintain the gate connection by increasing the surface area of the gate pad.
2) Attachment of all spacers to the PCB using SAC305 (T_{melt} = 214°C).
3) Formation of solder bumps on gate and source pads on one side of the PCB (say side-1) by using TS391AX (T_{melt} = 183°C).

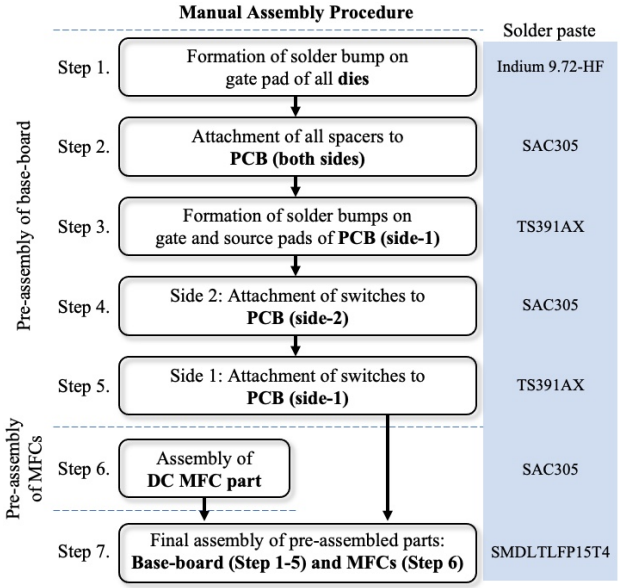


Fig. 5: Flowchart of the procedure of manual manufacturing for fabricating lab-scale prototypes.

4) Attachment of switches to the other side of the PCB (say side-2) by using SAC305.
5) Attachment of switches to side-1 by using the previously-formed bumps (TS391AX). During this process, the previously-populated switches on side-2 are held in position by using high-temperature Kapton tape.
6) Assembly of the decoupling capacitors and the DC MFCs using SAC305.
7) Attachment of the AC MFC and pre-assembled DC MFC using SMDLTLFP15T4 (T_{melt} = 138°C).

For ease of manufacturing, PCBs with copper-filled vias are preferred as they prevent leakage of solder paste through the vias during steps 3-5 above. Furthermore, filling the vias also reduces the thermal resistance of the via path, which enhances thermal performance by allowing more balanced DSC.

It is worth mentioning that the above-described process represents a manual assembly procedure, suitable for fabricating lab-scale prototypes. Considerable reduction of manufacturing complexity is possible by adopting a more systematic assembly process involving auxiliary stencils, fixtures and high-precision pick and place machines. Specifically, the use of the equipment and stencils would ensure reliable attachment of both gate and source pads of the dies onto the PCB and also allow simultaneous attachment of dies and spacers on the same side of the PCB in a single step. This would obviate the need for creation of solder bumps in steps 1 and 3 and thus the high-Pb solder paste in step 1. Furthermore, the use of fixtures would make it possible to hold all previously-soldered components present on the bottom side of the PCB [35], thereby allowing the use of the same solder pastes on the top side. Thus the assembly would be completed in less number of steps and need only two types of pastes - i) SAC305 for attachment of the dies, spacers and capacitors and ii) SMDLTLFP15T4 for attachment of the MFCs.

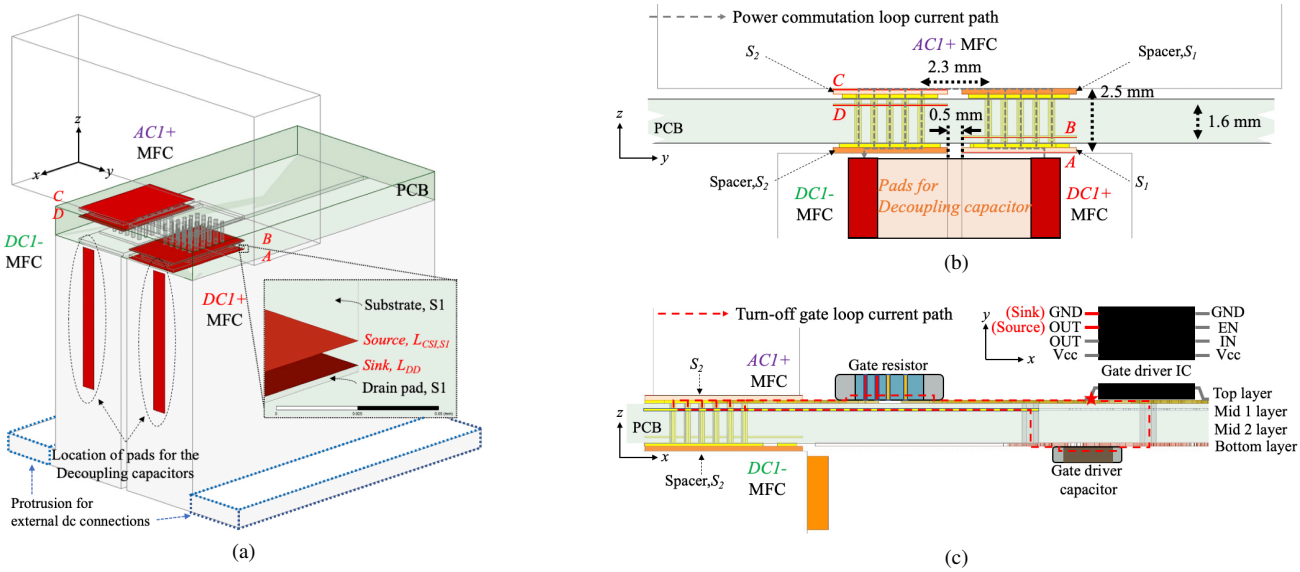


Fig. 6: Detailed structure of the proposed module. (a) Perspective view highlighting location of different source and sink planes (A-D, corresponding to Fig. 7a) for separation of power loop inductance components using Ansys Q3D Extractor. (b) YZ projection of the model with detailed dimensions. The high-frequency power commutation loop current flow path is illustrated. (c) XZ projection of the model illustrating the turn-off gate loop current path.

C. Reliability-related Considerations

While the proposed module design eliminates all wire bond-related failures, an added reliability consideration is thermo-mechanical stresses arising from coefficient of thermal expansion (CTE) mismatches. In particular, such stresses can arise at two joints within the assembly - i) between the SiC die and the PCB, and ii) between the die and the MFC. Though a detailed investigation into such reliability concerns is beyond the scope of this paper, it is worth mentioning that each of these stresses can be addressed by adopting suitable methods recommended in literature. For instance, stress on the first joint can be mitigated by adopting flip-chip attachment techniques such as use of solder spheres with underfill [16]. Furthermore, use of low-CTE PCB substrate materials like the ceramic-fiber enforced PCB material [36] is helpful to further mitigate the CTE-related concern. Likewise, the thermo-mechanical stress between the dies and the MFCs can be alleviated by using intermediate CTE buffer elements like copper-tungsten and molybdenum spacers or silver-loaded silicone [28]. Lastly, high-temperature PCB materials like TG170 and Polyimide laminate and prepreg materials should be preferably used in high heat-flux applications. The glass transition temperature of these materials are 170°C and 250°C respectively, which can help the substrate withstand high temperature variation of SiC devices, compared with general FR4 materials like TG140, used for low power applications.

D. Safety and Isolation-related Considerations

Use of electrified heat-sinks (MFCs) in the proposed switch module structure has several interesting implications. In conventional power switching device designs, the heat sink is isolated from power terminals and often connected to ground (protective earth) for safety considerations. Grounding the heat-sink also helps to reduce radiated electromagnetic interference (EMI) [37]. However, a grounded heat sink also

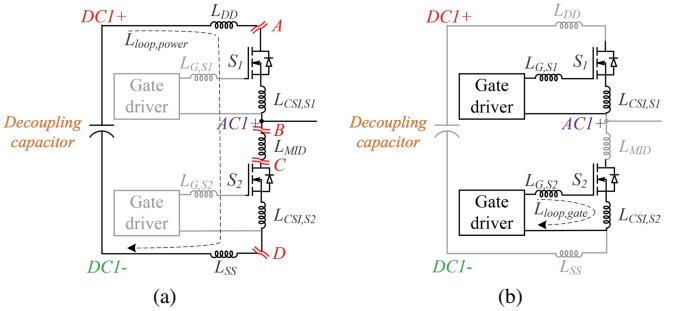


Fig. 7: Schematic of the half-bridge with separate parasitic inductances. (a) Power loop with distributed inductances and locations of physical cuts (A-D) for performing loop inductance separation using Ansys Q3D. (b) Gate loop.

increases conducted EMI noise [38], [39] by providing a path for common-mode (CM) currents to flow in the ground circuit. To alleviate this, connecting the heat-sink to the DC+/DC- bus-bars has been suggested by some researchers [38], [40] as this leads to the CM current circulating locally. Notwithstanding the associated benefits, such design approaches and all designs employing MFCs admittedly entail safety-related concerns. However, as discussed in [41], it is possible to address these concerns by providing adequate clearance between the electrified parts and external chassis/enclosure using isolation spacers and making them inaccessible using insulation film or coating [42]. As an example, for the converter implementation in [32], the 3D-printed, plastic fan housing provides added electrical insulation between the MFCs and the chasis.

III. Modeling of High-Frequency Parasitics

Switching performance of a high-frequency power module is strongly affected by parasitics like power and gate loop inductances, ac resistances and layout capacitances. Values of these parasitics were estimated by conducting 3D finite element analysis (FEA) simulations using Ansys Q3D-Extractor on the physical model of the switch module, shown in Fig. 6.

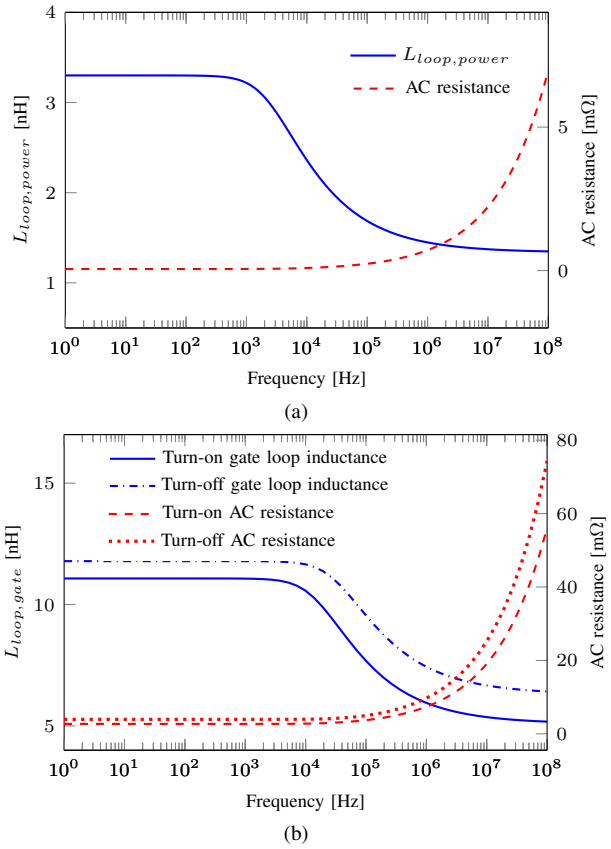


Fig. 8: Q3D-extracted values of total loop inductance and AC resistance with varying frequency. (a) Power loop. (b) Gate loop.

A. Estimation of Power Loop Inductance

Power loop inductance ($L_{loop,power}$) is one of the critical parasitic elements impacting switching performance. As shown in Fig. 7a, it is the inductance of the current commutation loop from the positive to the negative terminal of the decoupling capacitor. In order to obtain its value, source and sink excitations were assigned in the Q3D model at the location of the pads of the decoupling capacitor. The clearance between the switches and the spacers, and the gap between the DC+ and DC- MFCs were set to be 0.5 mm, as illustrated in Fig. 6b. A 6×5 symmetric via configuration was used in the model, and the distance between the leftmost via row for S_1 and the rightmost via row for S_2 was set to be 2.3 mm. Variation of $L_{loop,power}$ with frequency is plotted in Fig. 8a. The results show that $L_{loop,power}$ at 100 MHz is 1.349 nH, which is an order of magnitude lower than the conventional lateral wire-bonded SiC-based half-bridge module in [16]. This can be attributed to the compact power loop of the proposed vertical design achieved through planar interconnection and exact overlap paths between the forward and return currents. In addition, the vertically profiled MFCs enable close attachment of the decoupling capacitors to the switches.

B. Impact of Design Variables on Power Loop Inductance

In addition to the distance between the switches and the spacers, other important design factors that determine $L_{loop,power}$ are : 1) distance between the innermost rows of the vias, 2) distance between the DC MFCs and 3) thickness of the board. Fig. 9 shows variation in $L_{loop,power}$ for change in these dimensions. As can be observed, $L_{loop,power}$ increases monotonically with increasing gap distances, explained by the fact that the magnetic flux area of the power loop increases. Thus, for the smallest value of $L_{loop,power}$, lowest possible values of the distances are desirable. In this context it may be noted that final selection of a suitable clearance between the DC MFCs should also take into account factors like electrical insulation requirement and manufacturability. For example, if there is no additional insulating substrate between the DC MFCs, the gap between them cannot be lesser than 0.4 mm, decided by the dielectric strength of air (3 kV/mm) and the peak operating voltage of the die (1.2 kV). Similarly, if a clearance of 0.5 mm between the DC MFCs presents manufacturability concerns, a wider clearance of 1.5 mm may be used. As shown in Fig. 9, this increases $L_{loop,power}$ only marginally (from 1.35 nH to 1.55 nH), and is thus expected to cause negligible deterioration of the switching performance.

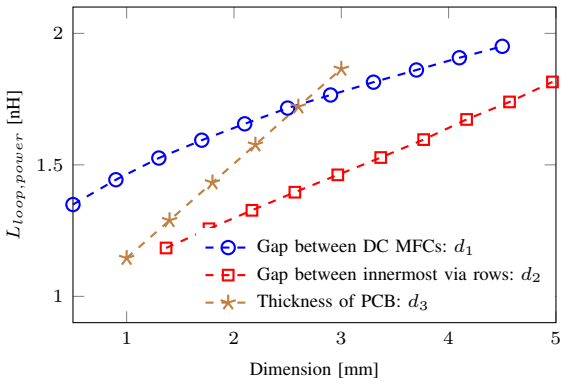


Fig. 9: Q3D simulation results showing variation of $L_{loop,power}$ with different dimensional variables. With varying d_1 (d_2 = 2.3 mm and d_3 = 1.6 mm). With varying d_2 (d_1 = 0.5 mm and d_3 = 1.6 mm). With varying d_3 (d_1 = 0.5 mm and d_2 = 2.3 mm). d_1, d_2 and d_3 are, respectively, gap between DC MFCs, distance between the innermost via rows and PCB thickness.

In summary, as Fig. 9 shows, the proposed module results in less than 2 nH of $L_{loop,power}$ for a wide range of design dimensions. Furthermore, if the dimensions are suitably minimized, this value can be reduced to even less than 1 nH, though this would require a relatively thin PCB (d_3 =1 mm).

C. Estimation of Power Loop Resistance

AC resistance (R_{ac}) of the power loop was also evaluated using Q3D and the results are plotted in Fig. 8a. It can be observed that in the sub-MHz range (the switching frequency range), R_{ac} is less than 1 mΩ, which is small in comparison to the on-resistance of the device (25 mΩ at $T_j = 25°$C) and thus the layout contributes negligible additional conduction losses. It is also important to estimate R_{ac} in the parasitic oscillation frequency range, since this relates to the damping of the switching oscillations. As seen from Fig. 8a, at around 100 MHz, R_{ac} is close to 10 mΩ.

D. Estimation of Gate Loop Inductance

Fig. 6c shows a simplified structure of the gate driver circuitry implemented in the proposed power module and the

corresponding gate loop path involving the gate resistor, source pad vias, Mid 1 layer, the gate driver IC decoupling capacitor and the driver IC itself. Like the power loop, the gate loop is also formed vertically through the PCB, which leads to reasonably small loop area and hence low inductance. Both turn-on and turn-off gate loop inductances and AC resistances were obtained using Q3D, and the results are shown in Fig. 8b. As shown, $L_{loop,gate}$ is about 5 nH and 6.5 nH for the turn-on and turn-off paths respectively at high frequencies, while the AC resistances are a few mΩ. It is noteworthy that coupling between the gate and power loops can be ignored since current flow in large parts of the two loops are orthogonal to each other (in YZ and XZ planes), as illustrated in Fig. 6b and Fig. 6c.

E. Estimation of Distribution of Power Loop Inductance

The total power loop inductance of the half-bridge can be divided into five components, as depicted in Fig. 7a. Each inductance has a different role in switching performance. To be specific, inductances from the interconnection path (L_{DD}, L_{MID} and L_{SS}) mainly affect the parasitic voltage ringing at switching instant, while common-source inductances ($L_{CSI,S1}$ and $L_{CSI,S2}$) significantly impact switching losses [43]. In order to extract the partial inductances of the loop, 0.01 mm thickness physical discontinuities are introduced within the 3D FEA simulation model, and source and sink excitations are assigned at the start and end locations of each part. Fig. 6a and 6b highlight the location of the source and sink planes, corresponding to the cut nodes (A, B, C and D) in Fig. 7a. All excitations are activated simultaneously to take the mutual effect into account. The values of the partial inductances at 100 MHz are listed in Table I, where the diagonal and off-diagonal terms denote self and mutual terms respectively. The sum of elements of each row gives the equivalent partial inductance of each part of the loop, considering the effects of mutual coupling with other parts. It should be noted that the total sum of elements of the obtained 5x5 matrix (0.8808 nH) is not strictly same as the previously-obtained value of $L_{loop,power}$ (1.349 nH). As discussed in [44], this is due to the inherently modeled equipotential excitations in Q3D, which prohibits an exact reflection of the realistic current flow. Despite this limitation, the partial inductance model is still valuable as it provides insights about distribution of the inductances within the power loop, which is vital to estimate behavioral characteristics of the half-bridge module.

It is noteworthy that the common-source inductances $L_{CSI,S1}$ and $L_{CSI,S2}$ in particular are quite low ($<$ 50 pH), which is helpful in improving switching behavior and reducing switching losses [45]. This can be explained by noticing that most of the return connection from the source of a switch to its gate-drive circuitry is completed through the inner PCB layer, adjacent to the layer on which the die is located. For instance, mid layers 1 and 2 are utilized for source-return connections for S_2 and S_1 respectively. Such a layout strategy thus effectively ensures a Kelvin-source connection [46] for the gate-drive, which lowers L_{CSI}. Another aspect worth highlighting is that the layout results in mutually orthogonal current flow in the gate and power loops, which reduces mutual inductance between the two loops and is thus beneficial for switching performance. The PCB-based packaging approach thus offers the designer several important advantages with respect to reduction of L_{CSI} and optimization of the layout of the gate loop, not always possible with DBC-based approaches.

TABLE I
Q3D-EXTRACTED VALUES OF PARTIAL INDUCTANCES OF THE POWER LOOP (in nH) AT 100 MHz.

	L_{DD}	$L_{CSI,S1}$	L_{MID}	$L_{CSI,S2}$	L_{SS}	Row sum
L_{DD}	0.0256	0.0023	0.0055	-0.0010	-0.0106	0.0218
$L_{CSI,S1}$	0.0023	0.0316	0.0210	-0.0034	-0.0134	0.0381
L_{MID}	0.0055	0.0210	0.3217	-0.0114	-0.0359	0.3009
$L_{CSI,S2}$	-0.0010	-0.0034	-0.0114	0.0343	0.0285	0.0470
L_{SS}	-0.0106	-0.0134	-0.0359	0.0285	0.5044	0.4730
Total sum						0.8808

F. Estimation of Layout Capacitances

Highly-compact, low-inductance switch modules may have high parasitic layout capacitances, which can significantly impact switching performance. For example, additional capacitance between drain and source ($C_{ds,layout}$) can impact zero-voltage-switching (ZVS) operation by making it harder to fulfill the energy criterion for ZVS. Similarly, stray capacitance between gate and drain ($C_{gd,layout}$) affects switching performance by coupling V_{ds} ringing on to the gate node due to Miller effect. Q3D simulations were performed to estimate the values of these capacitances, and the obtained values for $C_{ds,layout}$ and $C_{gd,layout}$ were 3.0395 pF and 3.1214 pF respectively. This indicates that the additional packaging capacitances are negligibly low in comparison to the intrinsic output capacitance of the selected switch ($C_{OSS} = C_{ds} + C_{gd} = 220$ pF at $V_{ds} = 1$ kV [47]). The low value of $C_{ds,layout}$ is made possible by the physical separation of the AC and DC MFCs to opposite sides of the PCB with minimum overlap area.

G. Spice Simulation Model

Analytical prediction of switching behavior of SiC devices is challenging due to non-ideal factors such as non-linear intrinsic capacitances, non-flat Miller plateau voltage and complex effect of the parasitics. SPICE simulations using manufacturer-provided device models and extracted parasitics can be an effective alternative approach and is considered in this work. Schematic of the LTspice simulation model is depicted in Fig. 10. As can be seen, the model also includes additional circuitry for capturing the effects of probe and oscilloscope (R_5, R_6, R_7 and C_4) as well as additional inductances (Ld_6, Ld_{12}) to reflect the remote location of the testing points on the PCB.

It is worth mentioning that distribution of inductances can result in significant discrepancy between the actual voltage across the switch and the measurement. To illustrate this, the measured drain-source voltage ($V_{ds,meas}$) across S_2 for a hard-switching transition is compared with the actual drain-source voltage ($V_{ds,actual}$) in Fig. 11. Two cases are considered with the same net sum of L_{mid} and L_{ss}, but different individual values. It is observed that the measured ringing amplitude is lower in the case when L_{mid} is higher, since the measurement

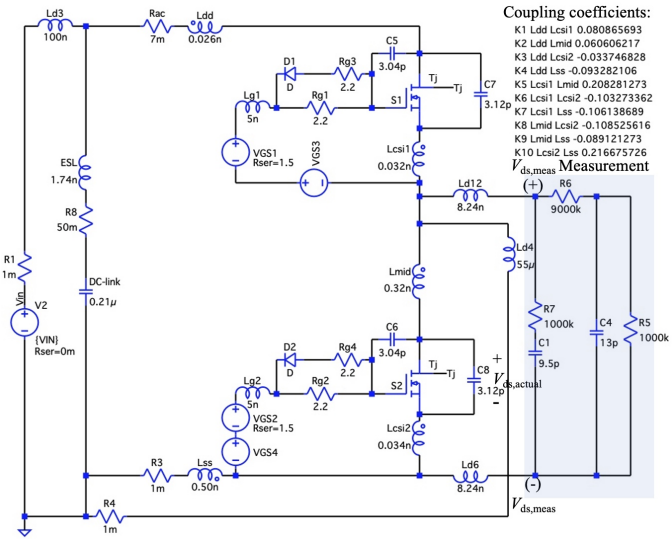


Fig. 10: Detailed LTspice simulation model including the Q3D-extracted parasitics (R_{ac}, $L_{loop,gate}$, C_{layout} and distributed $L_{loop,power}$ inductances) and manufacturer-provided device model. The parasitic elements are based on the ideal design, discussed in Section III, with the mutual inductances implemented by using coupling coefficients between the partial inductances. The parasitics are rounded to show two effective figures below decimal point. Measurement circuitry for measuring the drain-source voltage of the bottom switch (S_2) are also considered.

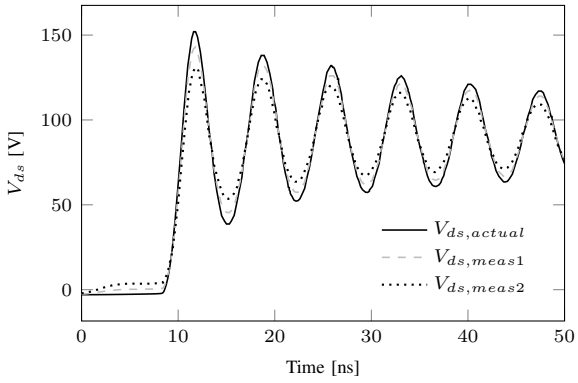


Fig. 11: Comparison between actual drain-source voltage of S_2 and the measured voltage across the testing points in LTspice simulation under a hard-switching condition (V_{in} = 100 V, I_L = 12.1 A). $V_{ds,meas1}$ is for case 1 with L_{mid} = 0.3009 nH, L_{ss} = 0.4730 nH, and $V_{ds,meas2}$ for case 2 with L_{mid} = 0.7009 nH, L_{ss} = 0.0730 nH.

loop contains L_{mid}. It is also interesting to observe that the actual drain-source voltage across the device can be higher than the measured value and the difference between them can be ignored only when L_{mid} is adequately low. The results thus demonstrate the importance of modeling the partial inductances within the power loop.

IV. Comparison with State-of-The-Art Approaches

A comparison of the proposed approach with other recently-reported, bare-die SiC-based, integrated switch modules, considering various aspects is presented in Table II. A comparative discussion on some of the key performance aspects is presented next to highlight the benefits of the proposed structure.

A. Comparison of Electrical Performance

The proposed switch module structure has extremely low $L_{loop,power}$ and reasonably low $L_{loop,gate}$. As mentioned earlier, this is possible due to i) the module's vertical loop structures, ii) close wire bond-less integration of the decoupling capacitors and gate-drive ICs and iii) the use of vertically-profiled MFCs, which enables compact electrical layout (in the X-Y direction) without compromising heat removal (in the Z direction). Moreover, as discussed in sections III-D and III-E, the use of PCB offers high design freedom for optimal layout of the gate-driver circuitry as well as the possibility of realizing a Kelvin-source connection with low coupling between the gate and power loops, leading to low common-source inductance. It should be mentioned that the PEP [18]–[20] and POL-based approaches [24]–[27] can also result in very low-inductance module designs, attributed to their structure with short distance between wide parallel conductor planes. However, this invariably leads to high parasitic capacitance between the drain and the source or gate of each switch (additional C_{oss}) [48], which can disrupt ZVS of switches [49] and thus be a bottleneck for high switching frequency operation. In contrast, the proposed approach mitigates this issue as it has much longer distance between the AC and DC nodes, since the corresponding MFCs are placed on opposite sides of the PCB. Furthermore, minimal overlap area between the AC and DC terminals due to the vertical shape of the MFCs also helps to reduce additional C_{oss}.

B. Comparison of Thermal Performance

Compared to the module configurations in [7]-[10], [13], [14], [20], [27], [16], the proposed structure enables quasi-DSC, which, as discussed in section II-B, can be enhanced by using copper-filled vias. While detailed thermal characterization of the module was not a focal point of the paper, preliminary experiments on a proof-of-concept prototype (cf. section V-E) demonstrate that under forced air-cooling condition each die can handle heat-flux exceeding 160 W/cm^2, corresponding to a thermal resistance of 1.8 K/W. CFD simulation results presented in [33] demonstrate that with liquid cooling a significantly lower thermal resistance of 0.3 K/W and a heat flux exceeding 500 W/cm^2 is achievable. Evidently, these numbers are indicators of extremely good thermal performance and more importantly, as mentioned in [33], the numbers are obtained with a much smaller heat-sink volume than most state-of-the-art approaches.

C. Comparison of Reliability

As mentioned earlier, the wire bond-less assembly of the proposed switch module serves to eliminate all wire bond-related reliability concerns present in [7]-[9]. However, as discussed in section II-C, the structure does have CTE-mismatch related reliability challenges, which may be addressed by following the suggested methods. The design of MFCs also impacts the reliability and thus further enhancements can be made by considering the effect of MFCs' geometry, shape and material on the reliability aspects. For example, an electro-thermo-mechanical co-optimization framework similar to the approach presented in [51] can be invoked at the design stage. In this context it may be pointed out that even DBC-based switch modules have CTE-related concerns which may lead

TABLE II
COMPARISON OF THE PROPOSED SWITCH MODULE WITH RECENTLY-PROPOSED BARE-DIE SIC-BASED INTEGRATED MODULES.

Reference	Wire bonds	$L_{loop,power}$ [nH]	$L_{loop,gate}$ [nH]	Heat removal	Substrate type	Description of Integration	Power loop	Additional C_{oss}
[7]	Yes	2.4 (simulated)	3 (simulated)	Single-sided	AlN DBC	Decoupling cap.	Lateral	Low
[8]	Yes	7.3 (simulated)	N/A	Single-sided	Al_2O_3 DBC	Decoupling cap., gate-driver	Lateral	Low
[10]	Yes	3.38 (simulated)	N/A	Single-sided	FR4 PCB/AlN DBC	Decoupling cap., gate-driver	Lateral	Low
[9]	Yes	3.4 (simulated)	N/A	Single-sided	Al_2O_3 DBC	Decoupling cap., gate-driver	Vertical	Low
[13]	No	4.5 (simulated)*	4.3 (simulated)	Single-sided	AlN DBC	Decoupling cap.	Lateral with planar interconnects	Low
[14]	No	1.6 (experimental)	6 (simulated)	Single-sided	Al_2O_3 DBC	Decoupling cap.	Lateral with planar interconnects	Low
[18]	No	2.09 (simulated)+++	0.012 (simulated)+++	Double-sided	FR4 PCB-embedded	-	Vertical	36%
[19]	No	2+(experimental)*	N/A	Double-sided	FR4 PCB-embedded	Decoupling cap.	Vertical	20%
[20]	No	0.86**(experimental)*	N/A	Single-sided	FR4 PCB-embedded with Al_2O_3 DBC	Decoupling cap.	Vertical	18%
[27]	No	1.4++(experimental)+++	20 (simulated)	Single-sided	Flexible board/DBC	-	Vertical	High
[16]	No	4.88*(experimental)	0.25 (simulated)+++	Single-sided	FR4 PCB	Decoupling cap.	Vertical	Low
[15]	No	12.33 (simulated)	8.07 (simulated)	Double-sided	FR4 PCB or DBC	Gate-driver	Lateral	Low
[17]	No	1.5 (simulated)+++	N/A	Double-sided	Epoxy-resin	Gate-driver	Vertical	Low
[24]	No	5 (experimental)*	N/A	Double-sided	DBC/AMB	-	Vertical	High
[25]	No***	7.5 (simulated)+++	N/A	Double-sided	Resin-molded heat-spreader	-	Vertical	High
[26]	No***	1.63**(simulated)+++	N/A	Double-sided	AlN DBC	Decoupling cap.	Vertical	High
[28]	No	8 (simulated)+++	4 (simulated)	Double-sided	PCoB	-	Vertical with MFCs	High
[29]	No***	N/A	N/A	Double-sided	PCoB	-	Vertical with MFCs	Low
This work	No	1.349 (simulated)	5.1 (simulated)	Double-sided	FR4 PCB	Decoupling cap., gate-driver	Vertical with MFCs	5%

* Value including ESL of decoupling capacitors. + Value for four half-bridge legs. ** Value for two half-bridge legs. ++ Value for eight half-bridge legs. +++ Value not considering placement of corresponding components. (e.g., capacitor for $L_{loop,power}$ and gate-driver IC for $L_{loop,gate}$)
*** Wire-bonds still present for connection to gate-drive circuitry.
Some parasitics are estimated from the information presented in each reference.

to delamination of copper and/or the ceramic substrate [29], [23]. Furthermore, as mentioned in section I, CTE mismatch also poses reliability concerns with all PEP-based designs as the dies are surrounded by the PCB material. To be specific, typical values of CTE for SiC die, copper and FR4 substrate (in the Z-direction) are 5 ppm/K, 18 ppm/K and 60 pm/K respectively and this mismatch generates thermo-mechanical stresses, which may lead to cracks or delamination on the dies and the dedicated inner connections to the dies [21].

D. Comparison of Manufacturing Complexity

Lastly, from the manufacturing aspect, assembly of the proposed module structure is relatively less complicated than the PEP and POL-based designs. This is because, unlike PEP and POL designs, the proposed switch module does not require specialized equipment for implementing PCBs with elaborate blind vias and accurately patterned overlay structures.

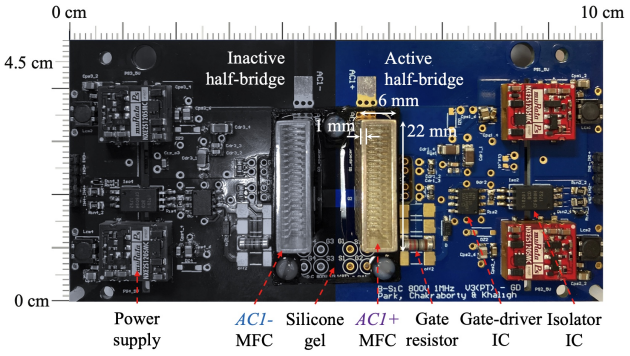
In summary, the proposed module design's important parameters and characteristics are at par or better than most state-of-the-art approaches while alleviating the trade-offs that existing works have. While the approach admittedly also has some challenges in aspects like reliability and isolation, these concerns can be addressed by adopting suitable mitigating measures, as discussed in sections II-C, II-D.

V. Experimental Results

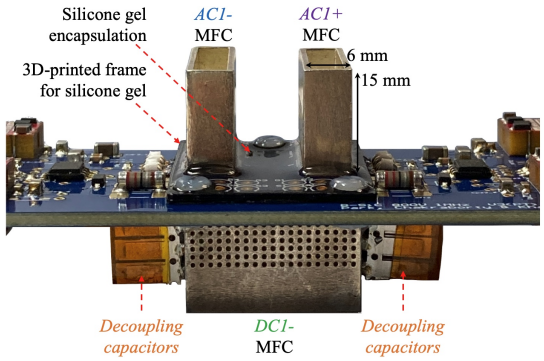
A. Laboratory Prototype

A laboratory-scale prototype of the switch module (Fig. 12) was fabricated to validate its operation. A full-bridge form of the configuration was implemented for use in a dual-active-bridge dc-dc converter [30], [31], and experiments were performed only on a single half-bridge part. 200 μm thick copper sheets were used as the spacers to keep the height same as the selected bare-die, whose thickness is 188 $\pm$ 40 μm. Automotive-grade Ceralink flex-assembly capacitors were adopted as decoupling capacitors due to their high capacitance density, low parasitics and high withstand temperature (150°C). The MFCs were realized using forced air-cooled, microchannel heat-sinks made of silver [33], with outer dimensions of $22\times6\times15$ mm^3. Details about their internal structure can be found in [33].

For ease of hand-assembly of the MFCs and capacitors, the prototype was designed with larger clearances than the ideal design (Fig. 6). In particular, the prototype had a clearance of 2.5 mm between the decoupling capacitors and the board, 3 mm between the switches and the spacers and 2.5 mm between DC+ and DC- MFCs. In contrast, for the ideal design, the aforementioned dimensions were only 0.55 mm, 0.5 mm and 0.5 mm respectively. As highlighted in Fig. 12b, the region surrounding the SiC dies was encapsulated by silicone gel to prevent potential dielectric breakdown through the air. A 3D-printed frame was used to ensure that enough amount



(a)



(b)

Fig. 12: Prototype power module in full-bridge form, used for experiments. (a) Top view of the prototype assembly (AC-side). (b) Zoomed-in front-view of the prototype highlighting silicone gel encapsulation within a 3D-printed frame and decoupling capacitors attached across the side walls of DC MFCs.

TABLE III
SPECIFICATIONS OF COMPONENTS USED IN THE PROTOTYPE.

Item	Part number	Description
Switch used	CPM2-1200-0025B bare-die	$V_{ds,max}$ = 1200 V, I_D = 98 A, $R_{ds,on}$ = 25 mΩ
Decoupling capacitor	B58035U9754M062	V_{rated} = 900 V, $C_{nominal}$ = 0.75 μF, ESL at 40 MHz = 1.74 nH
Gate driver power supply	NXE2S1215MC NXE2S1205MC	12 V - 15 V, 2 W; 12 V - 5 V, 2 W; $C_{isolation}$ = 2.1 pF
Gate driver IC	IXDN614SI	4.5 V $\leq$ Vcc $\leq$ 35 V, $I_{out,peak}$ = 14 A
Silicone gel	SEMICOSIL 915-HT	Dielectric strength $>$ 23 kV/mm

of gel was applied. Two low-isolation capacitance gate-drive power supplies were used for each switch to generate turn-on and turn-off gating voltages of +15 V and -5 V respectively. Considering use of the proposed switch module in high heat-flux applications, high-temperature Polyimide material (85N, Arlon [52])-based PCB was used for the area around the core switch module, and a separate TG170 FR4-based PCB was used for the gate-driver circuitry part. Detailed specifications of the components used in the prototype are listed in Table III.

B. Double-Pulse Test Results

In order to validate the switching performance of the module and characterize the layout-related parasitics, double-pulse test (DPT) was performed using a 55 μH clamped inductive load.

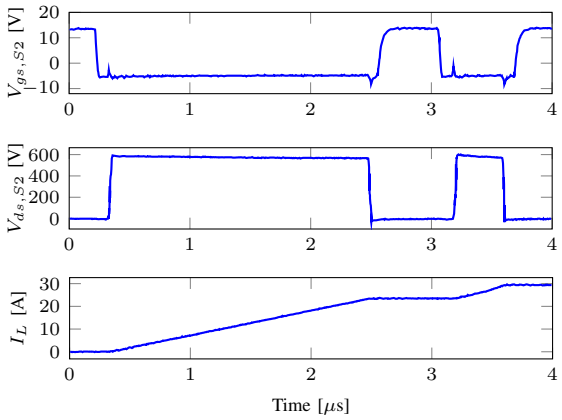


Fig. 13: Experimental waveforms of double-pulse test at V_{in} = 600 V. Traces from top to bottom are the gate-source of the low-side switch ($V_{gs,S2}$), drain-source voltage of the low-side switch ($V_{ds,S2}$) and inductor current (I_L).

Fig. 13 shows experimental waveforms of DPT at V_{in} = 600 V, in which gate and drain voltages of the bottom switch (S_2) and the inductor current were probed. The measurements were conducted using a 500 MHz voltage probe (P5100A, Tektronix) and a 30 A current probe (TCP0030A, Tektronix) on a 350 MHz oscilloscope[1] (MSO4034B, Tektronix). It was not possible to estimate the gate loop inductance through experiments due to the fact that the sum of internal gate resistance of the switch (= 1.1 Ω) and output resistance of the gate driver IC (= 0.8 Ω) was already close to the critical damping resistance (= $2\sqrt{L_{loop,gate}/C_{ISS}}$). Therefore, no distinguishable oscillations on the gate voltage were observed.

C. Measurement of Power Loop Inductance

Fig. 14 shows the waveforms of bottom-switch drain-source voltage at the hard-switching instant for three different input dc voltages: 50 V, 100 V and 150 V. According to the results, the corresponding oscillation frequencies (f_{osc}) are 85.5 MHz, 100 MHz and 110 MHz respectively. The total loop inductance ($L_{loop,total}$) including ESL of the decoupling capacitor can be calculated by

$$L_{loop,total} = \frac{1}{(2\pi \cdot f_{osc})^2 \cdot C_{oss}}. \quad (1)$$

The power loop inductance $L_{loop,exp}$ of the assembly excluding ESL is then calculated by subtracting ESL from $L_{loop,total}$, with the ESL value obtained from the impedance curve in [53], by noting the resonant frequency. Table IV lists the values of $L_{loop,exp}$ at different frequencies, which are around 3.6 nH. This number is higher than the FEA-based estimate of 1.35 nH for the ideal design, obtained in section III-A, which can be attributed to the larger clearances in the prototype than in the ideal design. To validate this hypothesis, an Ansys Q3D model was re-created with exact dimensions of the prototype itself. The experimental and simulated values of power loop inductances match closely, as seen by the

[1]Experiments were also performed by using a 1 GHz oscilloscope (DSOX4104A) and compared with the results from MSO4034B. Apart from minor variation in the ringing amplitude (less than 5% difference), no significant differences in ringing frequency and amplitude were observed, thereby validating the fidelity of the measurement.

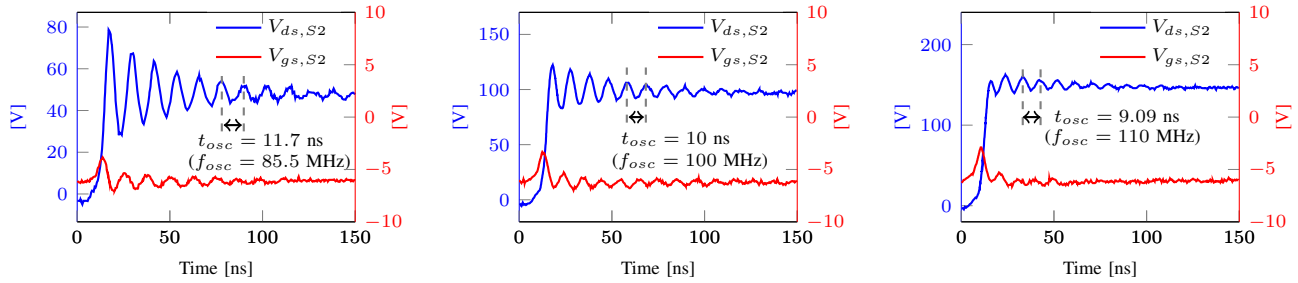


Fig. 14: Measured gate and drain voltage waveforms of the bottom switch during hard-switching transition of the top switch for different input voltages and inductor currents. (a) V_{in} = 50 V (I_L = 2.75 A). (b) V_{in} = 100 V (I_L = 5.6 A). (c) V_{in} = 150 V (I_L = 8.41 A).

TABLE IV

COMPARISON OF EXPERIMENTALLY MEASURED POWER LOOP INDUCTANCES ($L_{loop,exp}$) AND Q3D-EXTRACTED VALUES ($L_{loop,sim}$).

V_{in} [V]	f_{osc} [MHz]	C_{oss} [pF]	$L_{loop,total}$ [nH]	$L_{loop,exp}$ [nH]	$L_{loop,sim}$ [nH]
50	85.5	640	5.414	3.670	3.707
100	100	472.5	5.361	3.617	3.705
150	110	392	5.341	3.596	3.704
390	138.9	248.1	5.292	3.548	3.703

TABLE V

Q3D-EXTRACTED VALUES OF PARTIAL INDUCTANCES OF THE POWER LOOP (in nH) OF THE EXPERIMENTAL PROTOTYPE AT 100 MHz.

	L_{DD}	$L_{CSI,S1}$	L_{MID}	$L_{CSI,S2}$	L_{SS}	Row sum
L_{DD}	0.5523	0.0312	0.0881	-0.0143	-0.2069	0.4504
$L_{CSI,S1}$	0.0312	0.0348	0.0349	-0.0032	-0.0248	0.0729
L_{MID}	0.0881	0.0349	1.4493	-0.0005	-0.0434	1.5284
$L_{CSI,S2}$	-0.0143	-0.0032	-0.0005	0.0367	0.0555	0.0742
L_{SS}	-0.2069	-0.0247	-0.0434	0.0555	1.1665	0.9470
Total sum						3.0729

comparison in Table IV. Distributed loop inductances of the fabricated prototype were also analyzed and their values are listed in Table V. Comparing these values with those of the ideal design listed in Table I, additional inductances mainly arise from L_{DD}, L_{SS} and L_{MID}.

It is interesting to note from Fig. 14 that the oscillation amplitude of $V_{ds,S2}$ decreases as the input voltage increases. To be specific, the peak-to-peak voltage amplitude for V_{in} = 50 V is around 50 V_{pp} while the values are 40 V_{pp} and 25 V_{pp} for V_{in} = 100 V and V_{in} = 150 V, respectively. Further, no significant oscillation is observed in Fig. 13 for V_{in} = 600 V. This behavior can be understood by analyzing the turning-on behavior of S_1. The turn-on event can be divided into four intervals: 1) turn-on delay, 2) current-rise, 3) reverse-recovery, and 4) voltage-fall [54]. During interval 2, when the gate-source voltage exceeds the threshold voltage, the channel current ($I_{channel}$) of the incoming switch (S_1) starts to rise until it reaches the switch node current I_L. During interval 3, the reverse-recovery current (I_{rr}) of the body-diode of the outgoing switch (S_2) increases the channel current to ($I_{channel}$ + I_{rr}), at which instant $V_{ds,S1}$ starts to fall. During this period, it can be assumed that other stray circuit resistances are comparatively low and the channel resistance of S_1 dominates

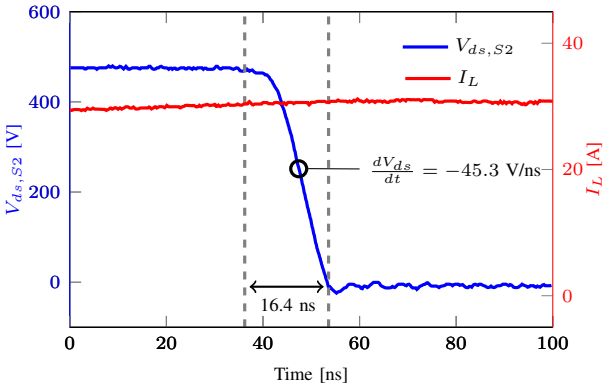


Fig. 15: Measured drain voltage of the bottom switch and inductor current at its ZVS turn-on instant at V_{in} = 480 V ($I_L \sim$ 30 A).

the equivalent resistance of the corresponding series RLC circuit. Due to the clamped inductive double pulse test set up, the value of I_L is proportional to V_{in}. Furthermore, the value of I_{rr} can be estimated to be approximately proportional to $\sqrt{I_L}$ [54], [55] and thus $\sqrt{V_{in}}$. This implies that higher input DC voltages are associated with higher overall $R_{ds,S1}$. Higher values of $R_{ds,S1}$ therefore increase the overall damping resistance of the power loop and thus oscillations of S_2 are more strongly damped for higher V_{in}.

D. Measurement of Layout Capacitance

In order to experimentally estimate additional layout capacitance between the switch node and the dc-rails, ZVS turn-on waveforms of the bottom switch were analyzed. Assuming an ideal case where the output capacitances of the top and bottom switches are given by $C_{oss,S1}$ and $C_{oss,S2}$ respectively, we have

$$\begin{aligned} I_L &= C_{oss,S1}\frac{dV_{ds,S1}}{dt} - C_{oss,S2}\frac{dV_{ds,S2}}{dt} \\ &= -(C_{oss,S1} + C_{oss,S2})\frac{dV_{ds,S2}}{dt}. \end{aligned} \tag{2}$$

In real implementation, the total output capacitance is composed by $C_{oss,S1}$, $C_{oss,S2}$ and $C_{ds,layout}$, so the total capacitance also can be obtained using the aforementioned voltage-current relationship. An example is demonstrated in Fig. 15 at V_{in} = 480 V. At the timing when $V_{ds,S2}$ becomes 240 V during the transition, both S_1 and S_2 have V_{ds} of 240 V and I_L of 30 A, and $dV_{ds,S2}/dt$ is -45.3 V/ns. Based on these values, the voltage-current relationship across the

TABLE VI
COMPARISON OF THEORETICALLY PREDICTED AND EXPERIMENTALLY MEASURED VOLTAGE TRANSITION TIMES AT ZVS TURN-ON.

V_{in} [V]	V_g [V]	I_{L0} [A]	$C_{eq,t}$ [nF]	$t_{ZVS,pred}$ [ns]	$t_{ZVS,exp}$ [ns]
480	0	30	0.847	14	16.4

capacitance predicts a total output capacitance of 0.662 nF. According to the datasheet of the selected switch, C_{oss} value at V_{ds} = 240 V is around 315 pF, so the datasheet-extracted total output capacitance of the half-bridge is 0.63 nF. The difference between the measured and the datasheet value is therefore around 5%, indicating that the fabricated module does not introduce significant additional capacitances between the switching node and the DC rails.

The result in Fig. 15 also validates the operation at high $dV_{ds,S2}/dt$ condition. As shown, the half-bridge prototype is operated at a $|dV_{ds,S2}/dt|$ of 45.3 V/ns without having any critical issues such as gate power supply isolation failure and additional C_{gd} oscillations.

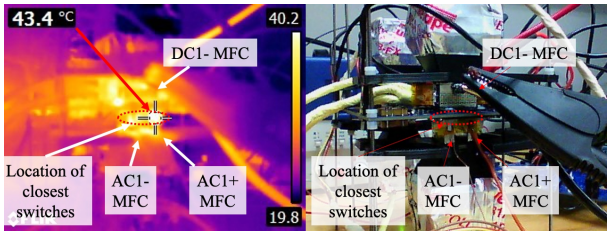
In order to further characterize the ZVS transitions, the time required for voltage commutation in Fig. 15 has been compared with theoretically predicted value, given by the following expression [56]

$$t_{ZVS,pred} = C_{eq,t} \int_0^{V_{in}} \frac{dv}{\sqrt{I_{L0}^2 + \frac{C_{eq,t}}{L}(2V_g v - v^2)}}, \quad (3)$$

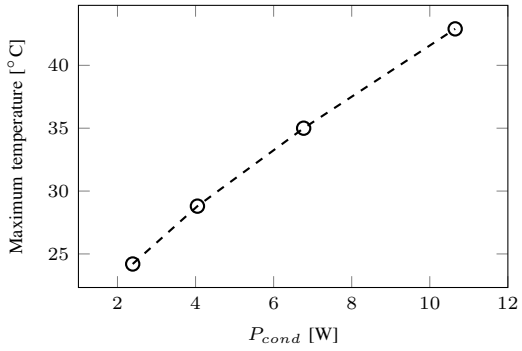
where $C_{eq,t}$ is the time-equivalent linear capacitance, I_{L0} is the initial inductor current, L is the inductance and V_g is the output dc voltage. Result of the comparison are listed in Table VI, which show good match between prediction and measurement. This result thus further validates the output capacitance characterization process.

E. Validation of Thermal Performance

Though the main focus of this work was on the electrical aspects, preliminary investigation into the experimental thermal performance of the module under forced-air cooling was also conducted using a dc conduction loss test. For this, high-side and low-side switches of both half-bridges were turned on and the total dc-link current was increased up to 30 A, by applying a small dc voltage ($\approx$ 1.5 V). Thus a dc current of 15 A was made to flow through each device, corresponding to a loss per switch of around 10.7 W and an associated heat-flux value of 41.1 W/cm^2 (= Loss per die / die area = 10.7 W / $(0.404 \cdot 0.644)$ cm^2). Two fans (9GA0312P3K001, Sanyo) were mounted on the top of the microchannel MFCs using intermediate funnel-shaped housing, one on each side of the full-bridge module. Thermal imaging result from an infrared camera under this condition is shown in Fig. 16a, while the average temperature of the two half-bridges for varying P_{cond} is plotted in Fig. 16b. As shown, under the maximum loss condition (10.7 W for each die), the temperature increased to 42.9°C from an ambient value of 23.6°C, which indicates that the junction-to-ambient thermal resistance ($R_{\theta,j,a}$) of each switch is around 1.8 K/W. It can be inferred that the prototype



(a)



(b)

Fig. 16: Forced-air convection: (a) infrared camera image at P_{cond} = 10.7 W. Two half-bridges were activated simultaneously for the experiment. The maximum temperature of the AC1+ MFC is 43.4°C. (b) Experimental results of the maximum temperature with varying P_{cond}.

itself can easily deal with upto four times higher loss (P_{cond} = 42.8 W) and heat-flux with the same air-flow setting, while maintaining the temperature of the dies below 100°C.

F. High Power Continuous Power Test

In order to further validate the performance of the module in a high-powered converter condition, a circulating power flow test was conducted by adopting a back-to-back connected non-isolated buck-boost circuit, illustrated in Fig. 17a. The test was conducted using a 2.5 μH external inductor (L_{load}), with the dc bus voltage at 480 V. The two half-bridge legs were operated with 50 % duty-ratio, 500 kHz switching signals, phase-shifted from one another to cause average power flow through L_{load}, similar to the principle of operation of a DAB converter. Since the two switching legs share the same dc bus, the power circulates back and forth between them, with the dc bus only supplying small residual losses. Fig. 17b shows key waveforms for a circulating power of 4.2 kW[2], where satisfactory high-frequency electrical behavior is observed as before. The estimated loss of each switch under the test condition was approximately 11.2 W and the temperature of the switches measured using a thermocouple increased to 44.0°C, demonstrating close agreement with the result obtained from the dc conduction loss test.

VI. Conclusions

This paper has discussed important characteristics of a bare-die SiC-based, wire bond-less, half-bridge power module with integrated decoupling capacitors, gate-driver circuitry

[2]Since each leg processes this power, the test condition corresponds to the full-bridge module processing 8.4 kW in an equivalent full-bridge DAB converter with two times higher leakage inductance (5 μH).

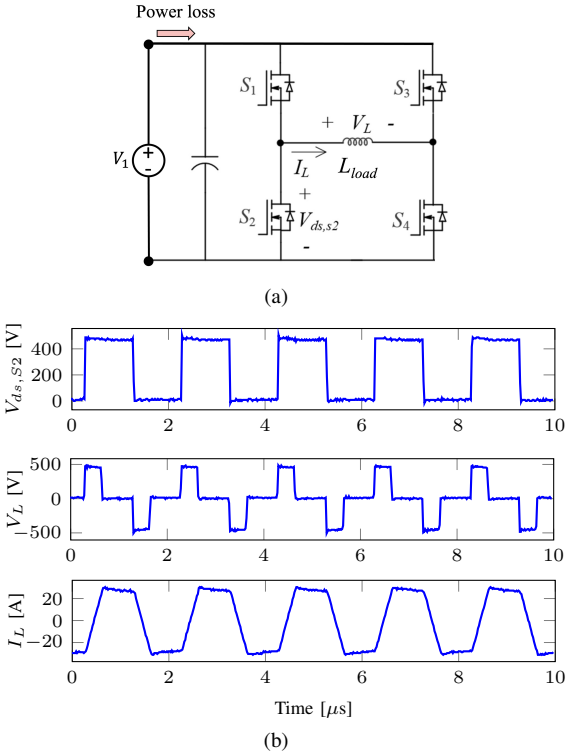


Fig. 17: Half-bridge DAB converter configuration with circulating power testing. (a) Schematic of the test setting. (b) Key waveforms.

and featuring MFCs, simultaneously acting as electrical busbars and heat-sinks. The proposed module can achieve improved switching performance due to its low loop inductances ($L_{loop,power}$ = 1.35 nH and $L_{loop,gate}$ = 5.1 nH at 100 MHz) attributed to its compact vertical loop structures, while introducing negligibly low parasitic capacitances. Therefore, the structure can be considered as a building block of high-frequency power electronics systems in EVs, including soft-switching converters (chargers) and hard-switching inverters. The use of PCB provides high design freedom to optimize the power layouts by making it possible to realize features like Kelvin Source connection. Detailed parasitic modeling is done using Ansys Q3D and validated using experiments on 600 V, 30 A laboratory prototype. The use of MFCs without involving TIM or ceramic substrate, demonstrates a potential enhancement in thermal performance due to direct DSC. Experimentally, the thermal resistance is found to be 1.8 K/W under forced air-cooling with microchannel coolers used as MFCs. The module also eliminates wire-bonding and DBC-related failures and its manufacturing is relatively less complicated than integrated modules involving elaborate overlay structures or PCB-embedded packaging. Future work can explore re-design of the module by addressing CTE mismatch concerns, implementing isolation barriers and EMI shielding, and pursuing more systematic, automated manufacturing.

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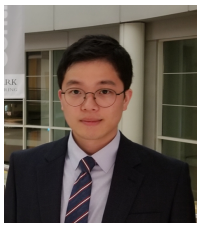

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