DAB Converter for EV On-Board Chargers Using Bare-die SiC MOSFETs and Leakage-Integrated Planar Transformer

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***Abstract*—This paper discusses electrical design optimization of a 3.3 kW, 380 V to 250-380 V, 500 kHz, dual-active-bridge dc-dc converter for on-board chargers, operated with constant-power (CP) charging. In order to operate the converter at 500 kHz without concerns on switching performance and efficiency while also improving power-density, a low-parasitics, PCB-based, wire-bondless full-bridge module featuring bare-die SiC MOSFETs and compact, electro-thermally multi-functional coolers is employed. High switching frequency operation also felicitates realization of the DAB inductor using the transformer's leakage inductance, thereby enhancing power-density by eliminating the need for a discrete inductor. Design strategy for such magnetic integration in a planar transformer is discussed followed by a systematic design optimization of the transformer, including selection of leakage inductance value, core geometry and number of turns for achieving zero-voltage-switching (ZVS) and maximum average efficiency over the entire charging profile. Experimental validation was performed using a proof-of-concept prototype, which is operated up to 3.3 kW and has a final projected power density of 5.44 kW/L. Results demonstrate operation with ZVS over the entire charging profile with satisfactory high-frequency waveforms and a peak efficiency of 98%.**

***Index Terms*—Dual-active-bridge, on-board charger, bare-die SiC MOSFET, planar transformer, power-density.**

I. Introduction

With the continuing global emphasis on transportation electrification, the demand for high power-density and high efficiency on-board charger (OBC) systems for electric vehicles (EV) has been growing significantly [2]. Typical structure of a single-phase, two-stage, isolated OBC system is illustrated in Fig. 1a. It consists of an ac-dc power factor correction converter stage for drawing high-quality current from the grid, followed by a dc-dc converter stage that regulates the battery voltage as well as provides high-frequency galvanic isolation. The focus of this paper is the dc-dc stage, whose key design requirements are high power-density and high efficiency over a wide range of battery voltage [3]. An additional desirable feature is that the dc-dc converter (as well as the dc-ac stage) should allow bidirectional power flow, since next-generation OBC systems are expected to have vehicle-to-grid (V2G) functionality to enable advanced grid support features like peak shaving and reactive power support [2].

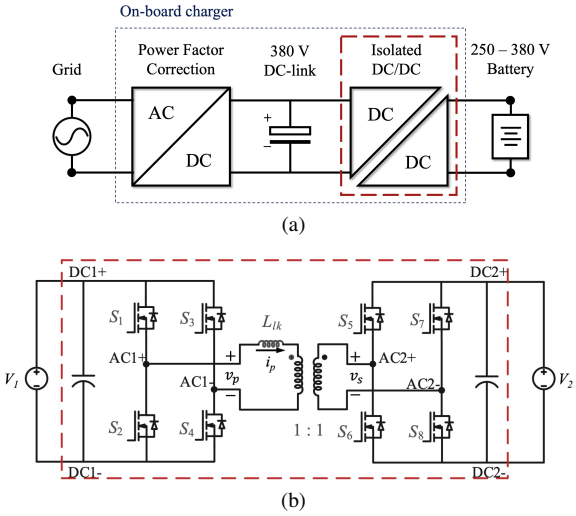

Fig. 1: (a) Block diagram of a two-stage, isolated OBC system. (b) Topology of DAB converter, considered for the isolated dc-dc stage in this paper.

Among various topologies reported in literature for dc-dc converters for OBCs, the LLC resonant converter [4] is a popular choice, which can achieve high power-density and efficiency due to possible zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) operation of its switches. However, the resonant tank of the LLC converter is inherently asymmetric, which operates as a series-resonant converter for reverse power flow and as such can only operate in buck mode [5]. While this can be addressed by using the bidirectional CLLC converter [6], which has a symmetric resonant tank, one challenge with the CLLC topology is that its efficiency can be poor when the switching frequency (f_s) moves far away from the resonant frequency [5]. To overcome this limitation, [5] proposed a new bidirectional, series-resonant converter topology to achieve high efficiency over a wide range of battery voltage. Another work in [7] proposed a uni-directional modified hybrid LLC converter, which is operated in different operation modes depending on the load and battery voltage to enhance efficiency. A common shortcoming of all of the aforementioned topologies is that the passive components of the resonant-tank, particularly the resonant capacitors, can add

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non-negligible volume, thereby impacting their power-density [8]. The resonant-transition, phase-shifted full-bridge (PSFB) converter [9] is another possible candidate topology which has the advantages of simple control, low reactive power flow and possible ZVS operation. However, it suffers from problems like duty-cycle loss, limited light-load efficiency and turn-off voltage spikes on the current-fed side devices.

The dual-active-bridge (DAB) converter, shown in Fig. 1b, has also been investigated as the dc-dc stage of both single-stage [10] and two-stage [11] OBC systems. This topology has advantages like capacitively-clamped operation of the switches, resulting in lower turn-off voltage spikes than PSFB topologies and possible zero-voltage-switching (ZVS) operation in both directions of power flow. Further, the DAB topology is inherently symmetric and compared to resonant-tank topologies, requires lesser passive components, which may be advantageous in terms of power-density [8]. Moreover, the DAB converter is normally operated at fixed f_s, which is an advantage compared to resonant topologies, which are mostly operated with varying f_s and necessitate wide frequency range, bulkier passive components and EMI filters [12]. The DAB converter also has its own challenges like high circulating power and possible loss of ZVS under light-load and non-unity voltage-gain conditions when operated with square wave modulation, referred to as single-phase-shift (SPS) modulation in this paper. These challenges can be addressed by either using widely-studied phase-shift-based modulation strategies [13] or adopting auxiliary circuitry such as additional resonant tank [14], inductor and switch pair [15], and the current-fed DAB structure [16]. Notwithstanding the limitations, in view of the other aforementioned advantages, this work explores the use of the DAB topology for the development of a high-performance dc-dc converter of a two-stage OBC system. The specifications of the converter are listed in Table I and the OBC is assumed to be designed to operate with the constant-power (CP) charging profile. Compared to other charging protocols like constant-current (CC), CP charging results in faster charging and better utilization of the power capacity of the charger [17]. While CP charging also has some concerns with regard to battery capacity fading [18], it is finally considered in this work because of its stated benefits.

In order to meet the above-stated objectives, three design strategies are pursued, the first of which is operation at a relatively high f_s. Operation at high f_s is a key enabler to enhance power-density by reducing the size of passive components, and for the present design, a value of 500 kHz is chosen. However, an important consideration with operation at high f_s is ensuring ZVS with low conduction losses to ensure good efficiency, which as mentioned earlier, can be challenging for a DAB converter used in charger applications. Unlike the previously-mentioned hardware-based approaches, this is addressed in the present work through combined design and modulation optimization, involving proper selection of values of L_{lk} and the phase-shift parameters. The other two design strategies relate to the key highlights of this work and involve 1) use of a unique full-bridge switch module featuring bare die SiC MOSFETs and 2) use of a planar transformer with high leakage inductance, which serves as the series inductance of the DAB converter (L_{lk} in Fig. 1b). For enabling fast and robust switching behavior, several bare-die SiC-based switch module design approaches with integrated gate-drivers and/or decoupling capacitors have been proposed recently [19]–[22], which can be advantageous in terms of the power-density due to their tight composition. However, these approaches either entail fundamental trade-offs between switching and thermal performance [21], [22] or involve wire-bonding [19], [20], which prohibits double-sided cooling and compromises reliability [23]. To mitigate these challenges, a unique bare-die SiC-based full-bridge switch module is used in this work, which results in enhanced switching as well as thermal performance. As discussed later in section IID, planar transformer structures with integrated leakage inductance reported in literature have limitations like unstable L_{lk} value [24], high values of parasitic capacitances and large footprint area [25], [26]. This work utilizes an integrated planar structure which do not have these limitations and can be considered a suitable candidate for high-frequency, high power-density applications. To summarize, the contributions of this paper are as follows:

- An electro-thermally integrated, compact, wire-bondless, bare-die SiC-based switch module featuring extremely low parasitics and double-sided cooling is implemented for high-frequency converter applications, and its performance is validated experimentally under powered condition in a 500 kHz DAB converter, working as the dc-dc stage of a 3.3 kW OBC.
- A systematic design procedure for selection of optimal value of L_{lk} and modulation parameters of the DAB converter is presented based on highly accurate analyses of converter operation and ZVS turn-on requirements. As a result, the converter operates with the minimum RMS value of transformer current (I_{rms}) while achieving ZVS during the entire CP charging stage, without requiring any auxiliary circuitry.
- Use of DC-bus voltage modulation in conjunction with converter modulation is proposed to realize ZVS with lowest I_{rms} under light-load conditions in the constant-voltage (CV) stage.
- A systematic approach towards efficiency-optimal design of a single-layer high-frequency planar transformer with integrated L_{lk} and extremely low parasitic capacitances is proposed by investigating the correlation between the physical design of the transformer and its electrical characteristics.

The rest of the paper is organized as follows. An overall description of the bare-die SiC-based full-bridge switch module and planar transformer implementation is presented in section II. Section IIIA discusses details of design analysis for

TABLE I
DESIGN SPECIFICATIONS OF THE DC-DC CONVERTER.

Item	Description	Item	Description
Maximum power	3.3 kW	DC-bus voltage (V_1)	380 V
Switching frequency (f_s)	500 kHz	Battery voltage (V_2)	250 - 380 V

identifying a range of L_{lk} based on the criterion of minimizing I_{rms}, while satisfying the energy-related ZVS criterion of the switches. Final design of the transformer, including an optimal selection of the value of L_{lk}, choice of core geometry and number of turns for achieving the highest efficiency, is outlined in section IIIB. Transformer design challenges for operation with CC charging are then highlighted, followed by a discussion on operation under light-load condition. Finally, details of the hardware prototype and experimental results are presented in section IV.

II. Overall Hardware Composition

A. Motivation for Use of Bare-die Switches

Selection of bare-die SiC MOSFETs, in contrast to normally used packaged discrete switches, is motivated by two design considerations. Firstly, as illustrated in Fig. 2, bare-die switches occupy significantly smaller footprint area than corresponding packaged devices and thus occupy smaller PCB real-estate, which can improve power-density. Secondly, discrete MOSFETs have substantially higher packaging inductance (due to internal bond wires and leads), which limits their switching performance and can lead to non-negligible switching losses at high f_s, even in converters with ZVS. As mentioned in [27], packaging inductances in a typical TO device are of the order of 10 nH, whereas that for a bare-die is only a few fH. Thus, switch modules built using bare-dies can have substantially lower power loop (L_{power}) and gate loop (L_{gate}) inductances than those with discrete devices. Such high values of L_{power} and L_{gate} can slow down switching transitions to the extent that turn-off losses could be significant at high f_s. Thus, even if a converter undergoes ZVS turn-on (as in a DAB), switching losses could limit its operation at high f_s if discrete devices are used.

B. Wire-bondless Full-bridge Module with Bare-dies

Overall structure of the bare die SiC-based full-bridge module is illustrated in Fig. 3. As shown in Fig. 3c, all switches are soldered on the printed circuit board (PCB) with their gate and source pads facing the PCB, and the top and bottom devices of a half-bridge are placed in diagonally opposite locations on either side of the PCB. Each source pad is connected to its corresponding ac-link or dc-link bus-bar (depicted by the white blocks) using through-hole-vias (THVs) and a thermo-electrically conductive spacer (made from copper) placed on the other side of the PCB. For example, the drain pad of S_1 is directly connected to the DC1+ bus-bar while its source pad is connected to the AC1+ bus-bar through corresponding THVs and the spacer of S_1. The AC1+ bus-bar makes a direct connection to the drain of S_2, whose source pad is connected to the DC1- bus-bar through its THVs and spacer. The ac bus-bar is finally connected to the transformer terminal through a copper trace on the PCB while the dc-link capacitors are connected across the dc bus-bars, as close to the PCB as possible. A similar wire-bondless interconnection approach is followed for the other half-bridge on the primary side (S_3-S_4) as well as the secondary side switches. The final assembled view of the module in Fig. 3d shows the location of the dc-link

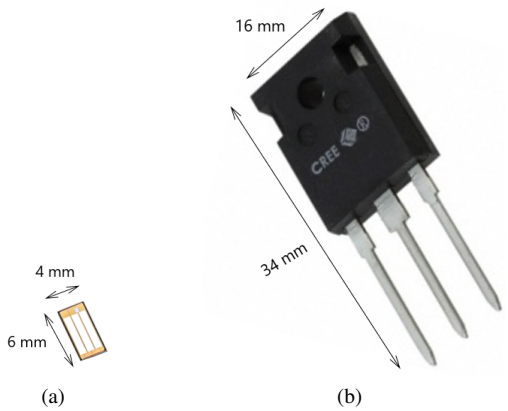

Fig. 2: (a) Dimensions of the bare-die SiC MOSFET considered in this work. (b) Dimensions of a discrete SiC MOSFET in TO-247 package.

decoupling capacitors as well as connections to the transformer and gate driver circuitries via PCB traces. For the proof-of-concept prototype in this work, 200 μm thick copper sheets are used as the spacers to keep the height of the bus-bars same as the selected bare-die, whose thickness is 188$\pm$40 μm. As an additional design strategy to mitigate possible thermo-mechanical reliability concerns due to coefficient of thermal expansion (CTE) mismatches, use of CTE-buffer elements can be considered instead of direct soldering of the dies and the bus-bars. For example, solder spheres with underfill material for the connection between the MOSFET dies and the PCB [28], and an intermediate molybdenum spacer [29] for the attachment of the bus-bars to the dies are possible solutions.

The layout of each half-bridge results in vertical loop design and thus low loop areas for both the power and gate loops. This leads to low values for the corresponding loop inductances and is thus expected to yield satisfactory high-frequency switching behavior. In addition, by placing the dc and ac bus-bars on opposite sides of the PCB, parasitic capacitance between switch nodes and dc rails is minimized, which, if large, can disrupt ZVS by increasing energy required for ZVS. FEA analysis indicates that the power loop inductance and the gate loop inductance could be as low as 2.2 nH and 5 nH at 100 MHz, and the layout capacitance between the drain and source of each switch is within 2% of the output capacitance of the switches. Further, the switch module arrangement not only improves electrical performance by significantly reducing loop inductances but also possibly enhances reliability by eliminating wire-bonds [23].

Another important feature of the switch module configuration is its multipurpose electro-thermal behavior. This stems from the fact that the bus-bars are made from metal like copper or silver, which have high thermal conductivity and can thus act as heat-sinks. Due to this dual behavior of the bus-bars as heat sinks, henceforth they are also referred to as multi-functional components (MFCs). As each switch is in contact with two MFCs, one directly and one indirectly through the THVs and spacer, the cooling capability of the arrangement can be described as quasi-double-sided (QDS). As shown in Fig. 3c, simplest realization of the MFCs is possible using metal blocks, cooled through natural convection. However, for higher loss applications forced-cooled heat-sinks with

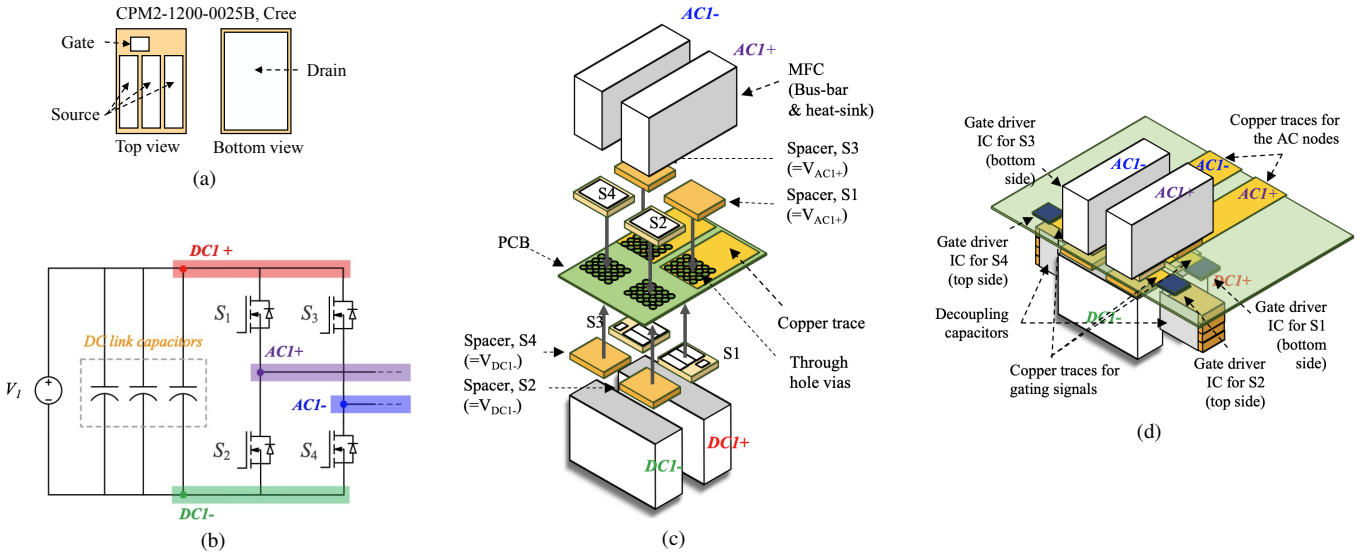

Fig. 3: Illustration of the switch assembly of the converter [30]. (a) Cartoon image of a typical bare-die MOSFET highlighting the gate (G), source (S) and drain (S) pads. (b) Schematic of one full-bridge. (c) Exploded view of the full-bridge assembly. Bare-die switches of each half-bridge are placed in diagonally opposite sides of the PCB with the G and S pads facing the PCB. Connections between the switches of each half-bridge is done using PCB vias, thermo-electrically conducting spacers and multi-functional components (MFCs) which serve as both bus-bars and heat sinks. (d) Assembled view showing location of the dc-link decoupling capacitors and connections via PCB traces to the transformer and gate driver circuitries. The arrangement ensures improved high-frequency electrical performance (due to low loop inductances) and improved thermal improvements (due to quasi double-sided cooling and absence of thermal interface material) in an ultra-compact volume.

similar outer geometry and having internal micro or mini-channels [30] can be considered. The hardware prototype in the present design uses a forced-air-cooled micro-channel cooler as the MFC, whose junction-to-ambient thermal resistance is approximately 1.9 K/W [31]. The QDS cooling feature of the arrangement coupled with the fact that electrical contact between the switches and the MFCs obviates the need for any thermal interface material (TIM), so thermal performance can be enhanced significantly. This further improves power-density by reducing the size of required heat sinks. For higher power applications or more aggressive cooling, liquid-cooled MFCs can be adopted. The CFD analysis results indicate that the junction-to-coolant thermal resistance using HFE7500 (Novec engineering fluid, 3M^{TM}) is approximately 0.3 K/W, which is significantly low [31]. Thus, the size of the MFC is expected to be reduced significantly if liquid cooling is employed for the same heat fluxes. For automotive applications, automatic transmission fluid (ATF) can also be considered as the dielectric coolant, since it is already present in vehicles [32].

C. Motivation for Use of High-L_{lk} Planar Transformer

As indicated before, the design strategy of using a transformer with high L_{lk} is motivated by the goal of elimination of an external inductor for realizing the series inductor of the DAB circuit. Such magnetic integration not only reduces part count and saves PCB space, but also potentially leads to reduction in losses by eliminating core and winding losses associated with a separate high-frequency ac inductor. In this context, it should be pointed out that such integration of the DAB inductor is in part facilitated by the design choice of high f_s. This is because average power in a DAB is inversely proportional to the impedance of the series inductor [10] and thus a higher f_s implies a proportionally smaller required value of series inductance, which can potentially be realized using the leakage inductance of the transformer. A planar transformer-based design is selected because of the advantages of controllable parasitics, low profile and better thermal performance associated with planar implementations.

D. Design Strategy for High-L_{lk} Planar Transformer

Several possible methods can be considered to realize high L_{lk} in planar transformers. The first approach, depicted in Fig. 4a, uses separate PCBs for the primary and secondary windings, which are separated with an intermediate high-permeability "magnetic shunt" element [24] for guiding the leakage flux. Another approach [26], shown in Fig. 4b, uses the center-leg of an E-core for the leakage flux path, and the primary and secondary windings are wound without interleaving around the two outer legs. A modification of this approach uses [25] interleaved windings with asymmetric number of turns on the outer legs, which results in reduced ac resistance. The value of L_{lk} can be adjusted by changing the air gap of the center-leg in [26] and/or changing the number of turns of the asymmetrical windings in [25]. A similar transformer structure in [33] utilizes partially-interleaved windings and realizes the leakage inductance through a horizontal air gap on one of the outer-legs. The last approach, shown in Fig. 4c, uses two separate PCBs for the two windings, which are physically separated to a much greater extent (than in Fig. 4a) with the effect that the leakage flux exists in the air gap between the windings. Operational difference of the aforementioned implementations are highlighted in Fig. 4d, 4e and 4f, which illustrate finite element analysis (FEA) simulation results for the magnetic field energy density of the different approaches. As can be observed, the leakage energies in the first and the second methods are almost entirely concentrated around the

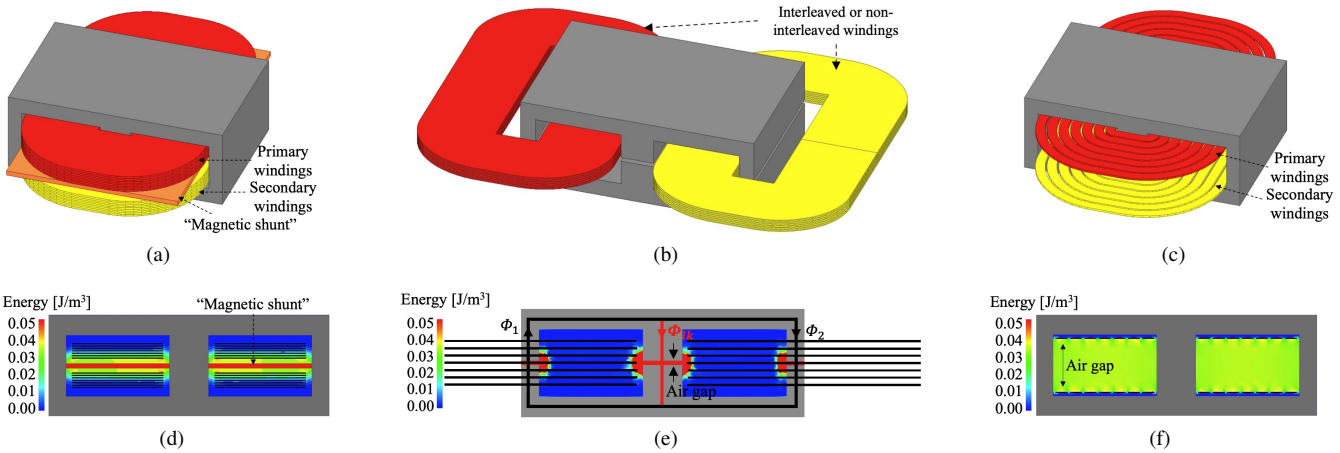

Fig. 4: Overall structure of considered transformer design options for high leakage inductance: (a) Design with physically separated windings and "magnetic shunt." (b) Design using center-leg for leakage flux. Either an interleaved-winding structure [25] or non-interleaved-winding structure [26] can be used for the windings of the structure. (c) Design with windings separated by a large air gap (finally selected). (d) Front view of (a) with FEA simulation results of energy density. (e) Front view of (b) highlighting flux paths. (f) Front view of (c) with FEA simulation results of energy density.

magnetic material, while in the last case the leakage energy is uniformly distributed across the air gap between the windings. While the first method is very effective at achieving high leakage inductance, it has the concern of possible variation in the value of L_{lk} due to the strong temperature dependence of the permeability of the "magnetic shunt" material. A shortcoming of the second approach is the large PCB space needed due to the portion of the windings outside the core, which reduces power-density.

Apart from the basic strategy of achieving enough leakage, differences are also possible with respect to the winding structure in the discussed methods. As shown in Fig. 4c, two separate single-layer PCB windings are used for the third method, as this helps maximize the distance between the primary and secondary windings and thus L_{lk} for a given core window height. In contrast, the other methods can use multiple-layer windings in general. While the use of multiple-layer windings can be potentially advantageous in terms of resistance due to the larger width/turn, it has some challenges too. One potential drawback is that it can result in high parasitic intra-winding capacitance (C_{intra}) in [24], [26] due to overlap across successive layers of the windings. This increases the required energy for achieving ZVS and can be a concern for the considered high-frequency DAB. Similarly, use of multiple-layers in [25] can result in excessive inter-winding capacitance (C_{inter}), due to overlap between the primary and secondary windings, which may lead to common-mode noise problems. Also, multiple-layer designs are not favorable from a thermal management perspective, as it can be challenging to extract heat from the inner layers of a multi-layer PCB. In view of the various design considerations discussed above, the single-layer structure in Fig. 4c is finally selected as it offers the benefit of realizing a stable and controllable value of L_{lk} with extremely low C_{inter} and C_{intra}.

III. Design of Transformer

In this section, details of design optimization of the transformer are presented, summarized by the flowchart depicted in Fig. 5. Under the given specifications, the transformer design

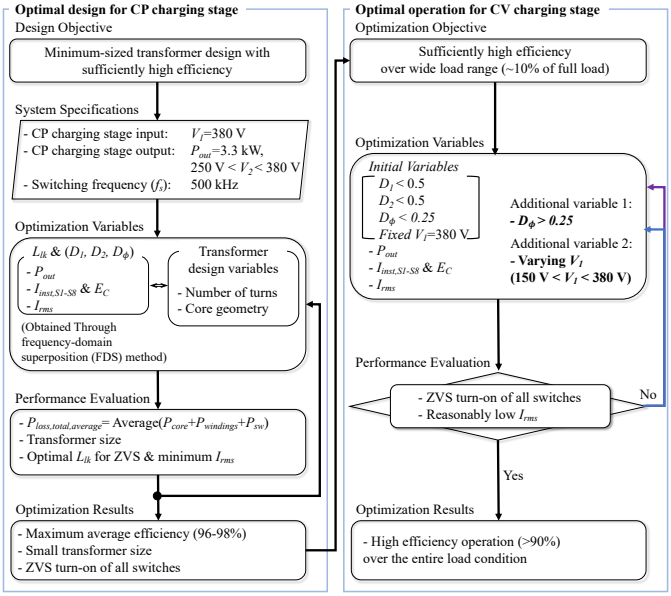

Fig. 5: Flowchart of the optimization procedure for the transformer design and modulation of the DAB converter.

aims for an optimal value of L_{lk} to ensure minimum losses as well as ZVS of all switches through comprehensive analysis of the DAB converter's operation. Furthermore, the correlation between the transformer design and the transformer's electrical characteristics is also investigated to minimize the footprint area while achieving maximum efficiency for CP charging stage. Finally, the operation at light load conditions in the CV charging stage is analyzed in detail, and an optimal modulation scheme is selected for sufficiently high conversion efficiency over the entire charging region.

A. Optimal Value of Leakage Inductance

Average power (P_{av}) of a DAB converter is given by (1a), where D_ϕ is the phase-shift between v_p and v_s, which can vary between 0 and 0.5. Considering the fact that the expression in (1a) is maximized for D_ϕ = 0.25 and proportional to V_1, V_2,

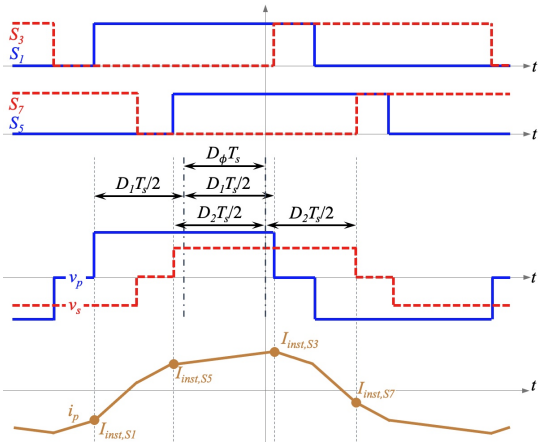

Fig. 6: Representative steady-state waveforms of transformer voltage and current highlighting the three modulation variables D_1, D_2 and D_ϕ.

TABLE II

EXPRESSIONS FOR $v_{p,k,pk}$, $v_{s,k,pk}$, $i_{k,pk}$ AND I_{rms}.

Term	Expression
$v_{p,k,pk}$	$\frac{4V_1}{k\cdot\pi}\sin(k\pi D_1)$
$v_{s,k,pk}$	$\frac{4V_2}{k\cdot\pi}\sin(k\pi D_2)$
$i_{p,k,pk}$	$\frac{1}{2k\pi f_s L_{lk}}\sqrt{v_{p,k,pk}^2+v_{s,k,pk}^2-2v_{p,k,pk}v_{s,k,pk}\cos(2k\pi D_\phi)}$
I_{rms}^2	$\sum_{k\ odd}^{2n-1}\frac{1}{2}I_{k,pk}^2$
I_{inst}	$\sum_{k\ odd}^{2n-1} I_{k,pk}\cdot\cos(k2\pi f_s t_{inst}+\theta)$

the maximum value of L_{lk} to ensure power flow $P_{av(max)}$ can be derived as (1b).

$$P_{av} = \frac{V_1 V_2 D_\phi(1-2D_\phi)}{L_{lk} f_s}. \tag{1a}$$

$$L_{lk(max)} \leq \frac{V_{1(min)} V_{2(min)}}{8 P_{av(max)} f_s}. \tag{1b}$$

For the converter specifications listed in Table I, $L_{lk(max)}$ is determined as 7.2 μH. The lower limit of L_{lk} is decided by the least possible value of ($D_{\phi(min)}$) of the employed microcontroller (MCU). This, in turn is related to the minimum power that can be transferred with maximum dc terminal voltages and is given by

$$L_{lk(min)} \geq \frac{V_{1(max)} V_{2(max)} D_{\phi(min)}(1-2D_{\phi(min)})}{P_{av(min)} f_s}. \tag{2}$$

Considering a minimum P_{av} of 1 kW, and a minimum achievable phase-delay time of 5 ns possible with the used TMS320F28335 MCU, $L_{lk(min)}$ is calculated as 0.72 μH.

While the DAB converter can be operated with any value of L_{lk} between the limits derived above in order to meet power transfer constraints, choice of the final value of L_{lk} is critical to ensure optimal efficiency. This is because, as mentioned in section I, for a wide range of battery voltage, the DAB converter can suffer from high conduction losses due to high transformer rms current (I_{rms}) and high switching losses due

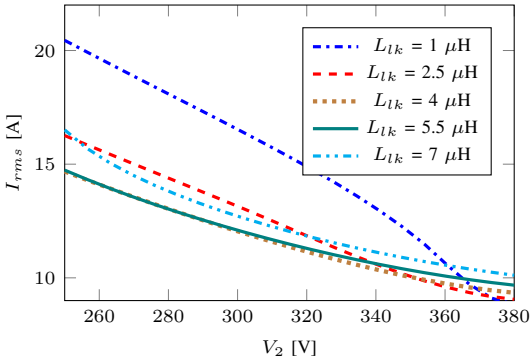

Fig. 7: RMS value of transformer current (I_{rms}) in the minimum RMS current-oriented modulation scheme as a function of V_2 with varying L_{lk} values. P_{out} is fixed at 3.3 kW for all cases.

TABLE III

EXPRESSIONS FOR TURN-ON INSTANT OF THE HIGH-SIDE SWITCHES.

Time	Expression	Time	Expression
$t_{inst,S1}$	$(-D_1/2-D_\phi)T_s$	$t_{inst,S3}$	$(D_1/2-D_\phi)T_s$
$t_{inst,S5}$	$(-D_2/2)T_s$	$t_{inst,S7}$	$D_2/2\cdot T_s$

TABLE IV

DIRECTIONAL REQUIREMENTS FOR ZVS TURN-ON OF SWITCHES

S_1 & S_2	S_3 & S_4	S_5 & S_6	S_7 & S_8
$I_{inst,S1}<0$	$I_{inst,S3}>0$	$I_{inst,S5}>0$	$I_{inst,S7}<0$
$I_{inst,S2}>0$	$I_{inst,S4}<0$	$I_{inst,S6}<0$	$I_{inst,S8}>0$

to absence of ZVS. The most common way to address these challenges is by adopting modulation strategies which vary the phase-shift between the switching legs of one or both bridges (e.g. S_1 and S_3 in Fig. 1b) [13]. Fig. 6 shows representative waveforms for operation with three such phase-shifts, commonly referred to as triple-phase-shift (TPS) modulation. As shown, D_1 and D_2 correspond to duty-ratios of v_p and v_s, respectively, and D_ϕ represents the phase-shift between the two voltages. Following the numerical optimization approach using MATLAB's "fmincon" function, outlined in [34], it is possible to find values of these three modulation variables D_1, D_2 and D_ϕ which minimize I_{rms} with or without ZVS consideration for a given battery voltage V_2 and charging power. The frequency-domain superposition (FDS) method greatly simplifies this approach by eliminating the complexity of analyzing different time-domain modes separately. The method proceeds by using closed-form expressions for peak values of the kth harmonic components of v_p, v_s and i_p, which are listed in Table II. Also listed are expressions for I_{rms} and the transformer current I_{inst} at a given time instant t_{inst}, which are used in formulating the RMS current minimization objective and ZVS constraints of the optimization problem respectively.

Results of the FDS-based numerical optimization script minimizing I_{rms} are plotted in Fig. 7, which shows variation in the minimum value of I_{rms} for varying V_2 and L_{lk}. As can be observed, I_{rms} is lowest for L_{lk} = 4 μH and tends to increase with increasing L_{lk}. However, low values of L_{lk}

TABLE V
ENERGY REQUIREMENTS FOR ZVS TURN-ON OF ALL SWITCHES IN DIFFERENT MODES

v_p	Condition	Switch	E_C	v_s	Condition	Switch	E_C
Square	D_1 = 0.5	S_1 & S_4	$-2Q_{OSS}(V_1)\cdot v_s(t_{inst})$	Square	D_2 = 0.5	S_5 & S_8	$-2Q_{OSS}(V_2)\cdot v_p(t_{inst})$
		S_3 & S_2	$+2Q_{OSS}(V_1)\cdot v_s(t_{inst})$			S_7 & S_6	$+2Q_{OSS}(V_2)\cdot v_p(t_{inst})$
Quasi-square	D_1<0.5	S_1	$Q_{OSS}(V_1)\cdot(+V_1-2v_s(t_{inst}))$	Quasi-square	D_2<0.5	S_5	$Q_{OSS}(V_2)\cdot(+V_2-2v_p(t_{inst}))$
		S_2	$Q_{OSS}(V_1)\cdot(+V_1+2v_s(t_{inst}))$			S_6	$Q_{OSS}(V_2)\cdot(+V_2+2v_p(t_{inst}))$
		S_3	$Q_{OSS}(V_1)\cdot(-V_1+2v_s(t_{inst}))$			S_7	$Q_{OSS}(V_2)\cdot(-V_2+2v_p(t_{inst}))$
		S_4	$Q_{OSS}(V_1)\cdot(-V_1-2v_s(t_{inst}))$			S_8	$Q_{OSS}(V_2)\cdot(-V_2-2v_p(t_{inst}))$

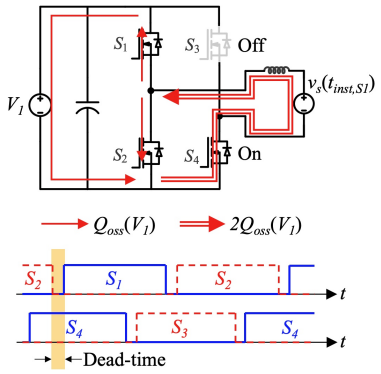

Fig. 8: Illustrating charge flow during the ZVS transition of S_1 when the primary-side transformer voltage (v_p) is a quasi-square waveform.

can disrupt ZVS operation by violating either of two basic requirements. Both of these conditions are related to the transformer current at the turning-on instant of each switch (t_{inst}), expressions for which are listed in Table III.

The first criterion is the necessary condition for achieving ZVS turn-on of a switch and requires that the switch current direction just prior to its turn-on should be negative, to be able to initiate voltage transition at the switch node. Corresponding conditions for each switch in terms of the instantaneous transformer current are listed in Table IV. The second criterion is the sufficiency condition for ZVS and requires that the energy stored in the leakage inductance (E_L) just prior to turn-on should be higher than the energy required to complete voltage transition of the capacitances (E_C) of the switching half-bridge under consideration.

Expressions for E_C for all the switches for different types of transformer voltage waveforms (square-wave or quasi-square wave) are noted in Table V, expanded from the analysis presented in [35]. In these expressions, $Q_{OSS}(V_i) = \int_0^{V_i} C_{OSS}(v)dv$ (i=1,2) represents the output charge of the switch under consideration, where $C_{OSS}(v)$ is the voltage-dependent, non-linear output capacitance of the switch. The transformer's primary and secondary voltages at the switching instant t_{inst} of the corresponding switch are denoted by $v_p(t_{inst})$ and $v_s(t_{inst})$ respectively. Fig. 8 explains an example ZVS transition of S_1 when v_p is a quasi-square waveform ($D_1 < 0.5$). Assuming S_1-S_2 to be the lagging leg, S_3 and S_4 are off and on respectively and the charge $Q_{OSS}(V_1)$ required for voltage fall of S_1 flows into V_1, which thereby consumes energy. $Q_{OSS}(V_1)$ is also required for voltage rise of S_2 and thus a net charge $2Q_{OSS}(V_1)$ flows out of the secondary-side reflected voltage ($v_s(t_{inst,S1})$), which thus supplies energy. Therefore, the total energy required to maintain the charge flow and complete the ZVS transition of S_1 is given by $Q_{OSS}(V_1)\cdot\big(V_1-2v_s(t_{inst,S1})\big)$, as listed in Table V.

Fig. 9 shows the modulation parameters that ensure minimum I_{rms} values, corresponding $I_{inst,S1}$ values, and the two energies (E_L and E_C) related to the ZVS requirement of S_1, for varying output voltage at three different L_{lk}: 4 μH, 5 μH and 6 μH. It may be noted that although analytical formulation of the constrained optimization problem considers generic TPS operation, the numerical optimization routine identifies SPS and dual-phase-shift (DPS) with inner phase-shift on the primary-side bridge as the optimal modulation schemes for operation under near-unity voltage-gain and low voltage-gain conditions respectively. Interestingly, if TPS modulation is forced (i.e. operation with SPS or DPS is actively precluded), it can be shown that it results in loss of ZVS operation (due to violation of the necessary condition for ZVS) of one leg on the secondary-side bridge as well as increased I_{rms} for low values of V_2.

It can be demonstrated that under the adopted modulation scheme, because of the step-down nature of the target operation (380 V to 250-380 V), the S_1-S_2 leg of the sending-end bridge is under more stringent condition for ZVS compared to the S_3-S_4 leg, since amplitude of switching instant currents of the former leg are always smaller. Further, it may be shown that under both SPS and TPS, the inductor's energy increases during voltage-transition of the receiving-end switches [35] since the energy for ZVS is drawn from the sending-end dc bus (V_1). From the preceding discussion it follows that there is no energy-related ZVS criterion for the receiving-end switches and evaluation of the ZVS condition for S_1 is enough to check for full ZVS of the converter. As can be observed from Fig. 9, L_{lk} = 4 μH does not satisfy the ZVS energy condition of S_1 at low voltages ($V_2 < 360$ V), while 5 μH and 6 μH achieve ZVS over the entire V_2 range. The minimum value of L_{lk} to ensure ZVS is determined to be 4.8 μH, which thus defines a lower limit for L_{lk} value. Within the determined upper and lower limits of L_{lk}, an optimal transformer design that provides the lowest total loss is explored next.

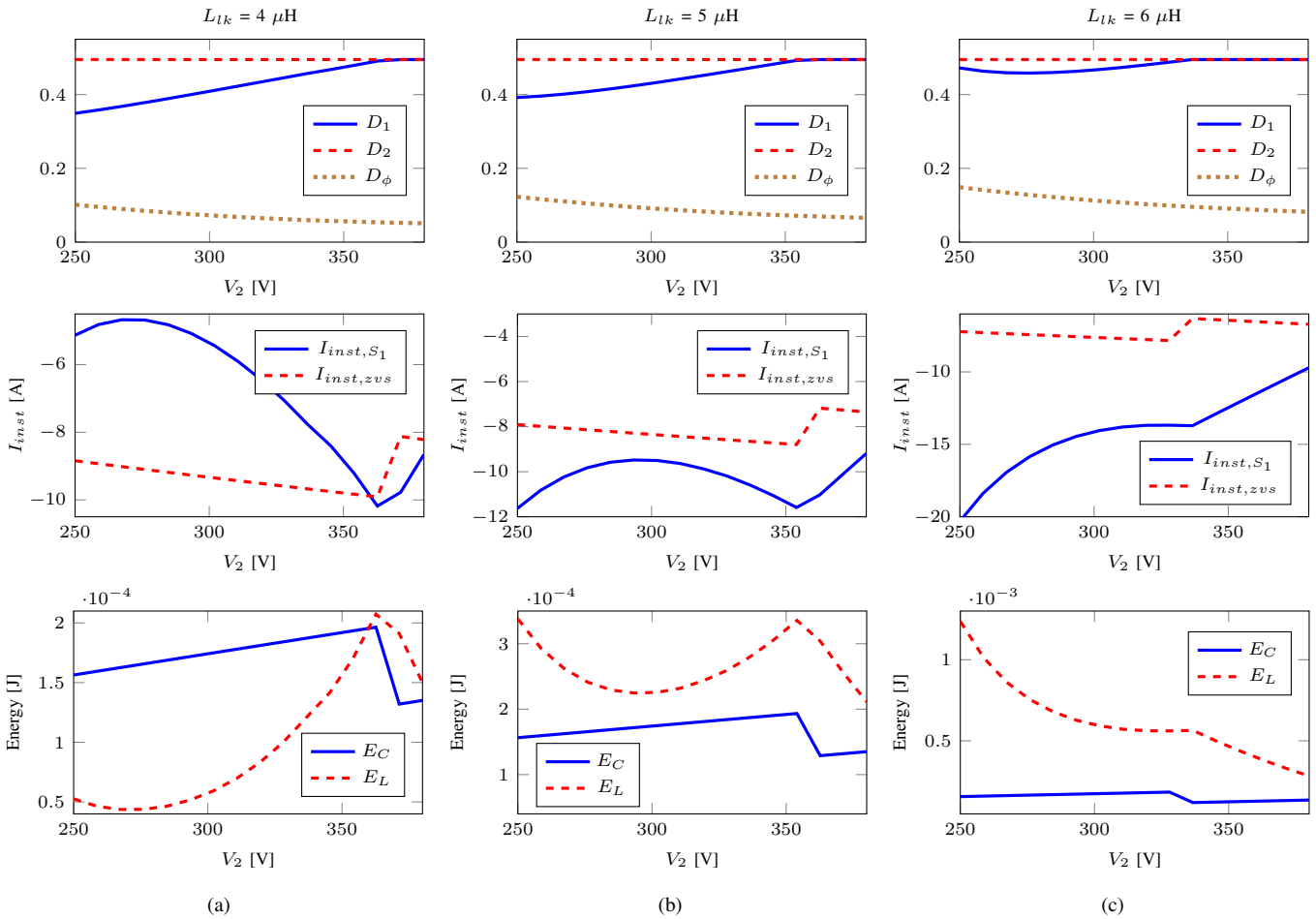

Fig. 9: (Top row) Trajectories of modulation parameters (D_1, D_2 and D_ϕ) that ensure minimum I_{rms} during CP charging stage. (Middle row) Current at turn-off instant and required current for ZVS turn-on of S_1, (Bottom row) Stored inductive energy (E_L) and energy required for ZVS turn-on of S_1 (E_C) with varying V_2. All plots are for CP charging with P_{out} = 3.3 kW. (a) L_{lk} = 4 μH. (b) L_{lk} = 5 μH. (c) L_{lk} = 6 μH. Only S_1 is evaluated in terms of the ZVS energy requirement as S_1 is under the most stringent condition for ZVS. It may be noticed that for L_{lk} = 4 μH, the ZVS energy criterion is not satisfied.

B. Feasible Range of Number of Turns

Based on the target minimum L_{lk} value of 4.8 μH identified in section IIIA, three different-sized E cores (E32, E38 and E58) are characterized in terms of the maximum obtainable L_{lk} values and ac resistances (R_{ac}) at 500 kHz, with varying number of turns (N). Fig. 10 shows the values of these parasitics, obtained from 3D FEA simulations[1] performed using Ansys Maxwell's Eddy current solver. The simulation results help identify the feasible range of N for each core, such that L_{lk} lies within the specified design limits. Specifically, the feasible range of N for each core correspond to those values such that $L_{lk} > L_{lk(min)}$ = 4.8 μH (to satisfy the ZVS limit) and $L_{lk} < L_{lk(max)}$ = 7.2 μH (to satisfy the maximum power transfer limit). It may be observed that among feasible designs, the value of R_{ac} is lowest for the largest core (E58) for $N = 7$ and thus this design choice is expected to result in lowest winding losses[2]. However, the core loss is expected to be high in designs with $N = 7$, as the magnetic flux density is inversely proportional to the number of turns.

In order to identify the optimal core geometry and number of turns, a detailed loss analysis is conducted. Three dominant loss factors are considered: transformer winding losses ($P_{winding}$), transformer core losses (P_{core}) and switch conduction losses (P_{cond}). Switching losses are assumed to be negligibly low, due to the low parasitics of the switch module and attainment of full-ZVS, which are validated through detailed LTspice simulations employing a realistic MOSFET device model provided by the manufacturer. P_{core} is calculated using the improved generalized Steinmetz Equation [36], while $P_{windings}$ and P_{cond} are obtained using FEA-derived R_{ac} and switch datasheet-derived $R_{ds,on}$ respectively, in conjunction with corresponding analytically-calculated RMS values of currents. Temperatures of windings ($T_{winding}$), core (T_{core}) and switches (T_{sw}) are assumed to be constant at 100°C,

[1]Referring to the guidance of the Generic Standard on Printed Board Design and PCB manufacturing capability (IPC-2221), the 3D model had 0.5 mm spacing for both the clearance between two adjacent winding traces and the distance from the cores to the outermost windings.

[2]With the same number of turns, larger cores have larger width per turn, thereby leading to lower dc resistance despite larger mean-length per turn. For example, each turn of the 7-turn with E58 cores design has a width of 2.486 mm, while that of the 7-turn with E38 cores design is 1.061 mm.

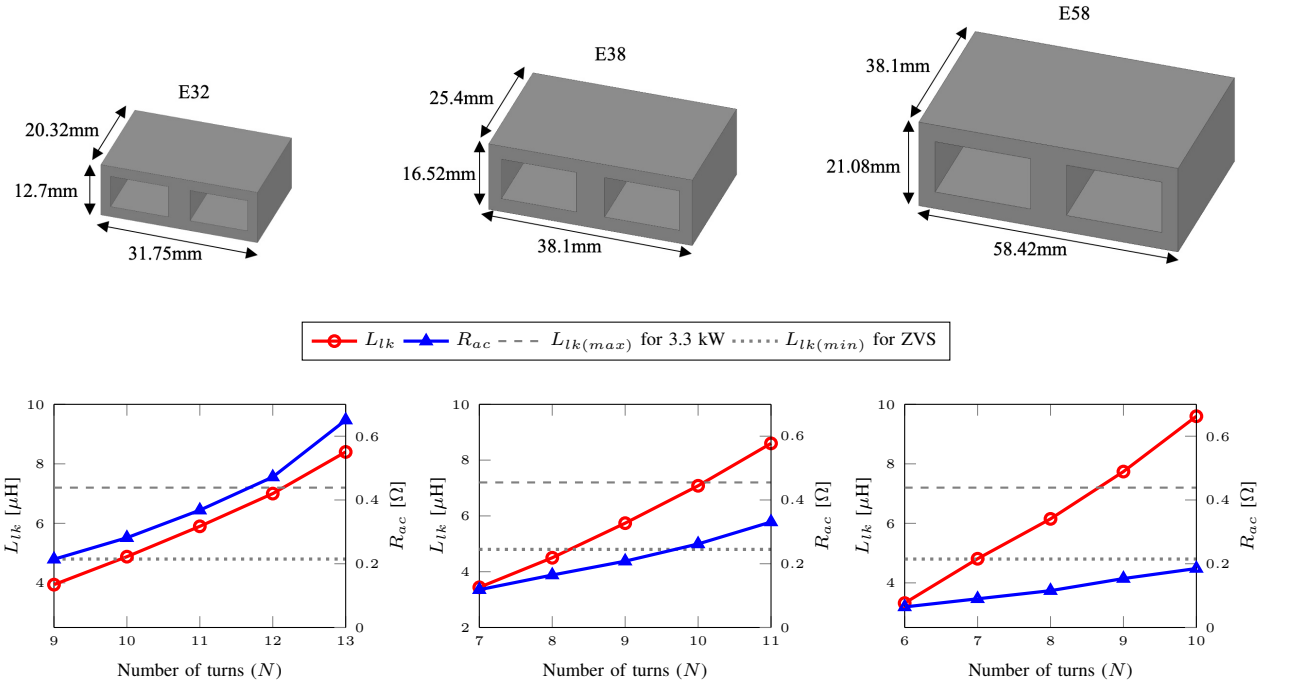

Fig. 10: Variation of maximum obtainable L_{lk} and corresponding R_{ac} (obtained using 3D FEA simulations) with varying number of turns (N) for three different core geometries. The R_{ac} values represent the ac resistance of one-side windings. Feasible range of N for each core corresponds to values such that $L_{lk} > L_{lk(min)}$ = 4.83 μH (ZVS limit) and $L_{lk} < L_{lk(max)}$ = 7.2 μH (power transfer limit). It may be observed that the value of R_{ac} in the feasible range is lowest for the largest size core (E58).

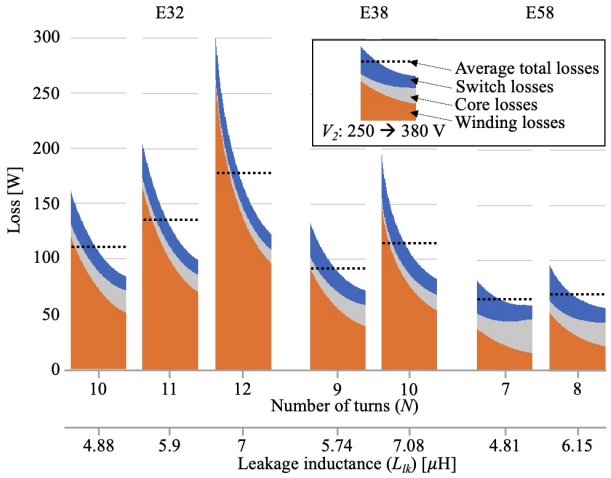

Fig. 11: Theoretical loss values for different transformer core geometries and corresponding feasible number of turns (obtained from Fig. 10). As explained in the inset, each plot shows variation of losses over the range of battery voltage (V_2) for CP charging at 3.3 kW. $T_{windings}$, T_{core} and T_{sw} values are assumed to be 100°C, 30°C and 50°C respectively. Highest average efficiency is obtained for the E58 core with $N = 7$.

30°C and 50°C, respectively, as they correspond to reasonable worst-case conditions for the losses. The estimation results are shown in Fig. 11, where each vertical plot shows variation of individual losses over the range of battery voltage for CP charging at 3.3 kW. As can be observed, the E58 core with $N = 7$ design has the lowest overall losses, so this design is finally selected. A related observation from Fig. 11 is that the maximum loss values of the transformer windings, core and

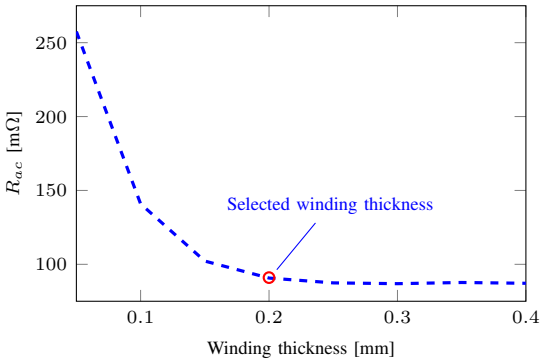

Fig. 12: R_{ac} variation with varying winding thickness for E58 with N = 7.

each switch are: $P_{windings,max}$ = 42.5 W at V_2 = 250 V, $P_{core,max}$ = 17 W at V_2 = 380 V, and $P_{sw,single,max}$ = 3.7 W at V_2 = 250 V respectively[3]. It should also be pointed out that the impact of winding thickness (t_w) on the value of R_{ac} is also evaluated by conducting FEA simulations using Ansys Maxwell's Eddy current solver for varying winding thickness. The results shown in Fig. 12 reveal that beyond a certain value of the thickness (around 0.2 mm), there is no remarkable reduction in R_{ac}. This can be explained by the fact that for high frequency operation, current tends to be concentrated on boundaries of a conductor due to skin and proximity effects. Therefore, a winding thickness of 0.2 mm is finally selected.

[3]These numbers are used to inform the design of appropriate cooling systems, detailed discussion on which is beyond the scope of this paper. The interested reader can find more details in [31] and [37].

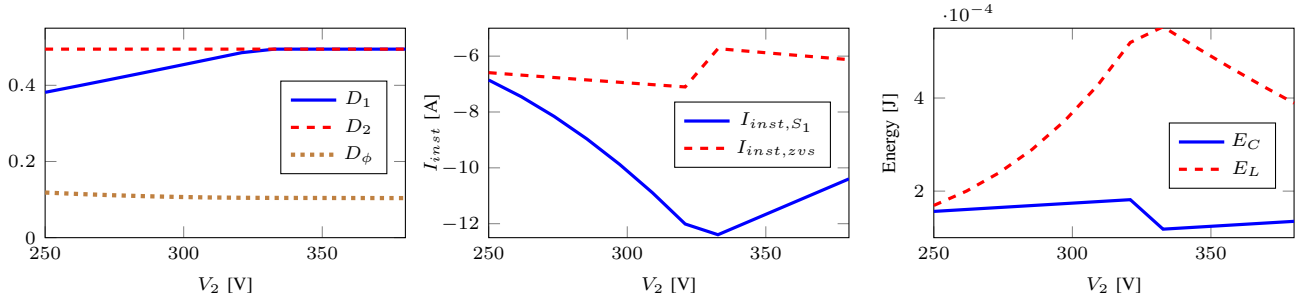

Fig. 13: Parameters at the minimum required L_{lk} for ZVS (=7.2 μH) under CC charging condition: (Left) Trajectories of modulation parameters (D_1, D_2 and D_ϕ) that ensure minimum I_{rms}. (Middle) Current at turn-off instant and required current for ZVS turn-on of S_1, (Right) Stored inductive energy (E_L) and energy required for ZVS turn-on of S_1 (E_C) with varying V_2. P_{out} increases proportionally with V_2, from 2.2 kW to 3.3 kW.

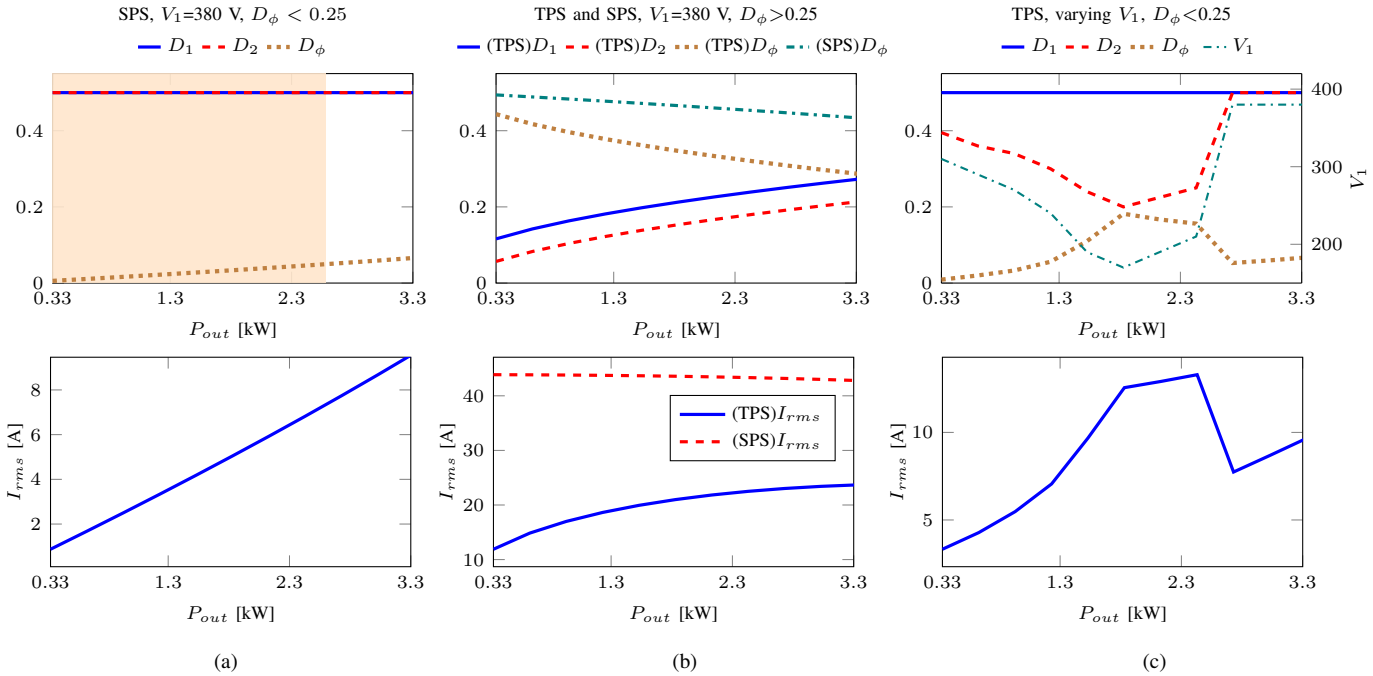

Fig. 14: (Top row) Trajectories of modulation parameters (D_1, D_2 and D_ϕ) that ensure minimum I_{rms} during CV charging stage for different modulation schemes. (Bottom row) Corresponding RMS values of transformer current. (a) SPS at fixed V_1 and $D_\phi < 0.25$. Partial-ZVS region is highlighted by the shaded orange zone. (b) TPS and SPS at fixed V_1 and $D_\phi > 0.25$. $D_1 = D_2 = 0.5$ for SPS. (c) TPS with varying V_1 and $D_\phi < 0.25$. 150 V is set as lower limit of V_1.

C. Impact of Charging Profile on Transformer Design

As discussed before, compared to CC charging process, a well-known advantage of CP charging process is faster charging since the maximum power period is longer [38]. Additionally, CP charging is found to be more advantageous for design of the DAB converter, especially when the leakage inductance serves as series inductance. This is because the overall current level of CC charging is lower than that of CP charging, especially at low P_{out}. The lower current level results in lower current values at the turn-off instant of switches and therefore the CC charging profile requires higher values of L_{lk} to meet the ZVS energy condition over the whole charging period. However, the maximum L_{lk} value is limited by the maximum power within a certain set of $V_{1(min)}$, $V_{2(min)}$ and f_s, as determined by Equation (1b). Even if it is possible to achieve ZVS with the L_{lk} value below the upper limit, as discussed in Section III, the transformer designs that can obtain higher L_{lk} values are associated with larger core geometry and/or higher R_{ac} value. To be specific, the minimum required L_{lk} value that ensures ZVS over the entire operational region of CC charging is 7.2 μH, as shown in Fig. 13. The design that can provide 7.2 μH is E58 core with 9-turns, whose R_{ac} value is 0.15 Ω (cf. Fig. 10c), which is more than 1.5 times higher than that of the optimal design for CP charging.

D. Operation Under Light-Load Condition

The concluding stage of a typical CP charging process is a constant-voltage (CV) phase, which continues until the level of state-of-charge (SOC) reaches to 100% [38]. During this stage, the transferred power decreases while maintaining the battery voltage V_2 at its peak value. Therefore, operation of the converter at maximum battery voltage with a widely varying P_{out} (from full-load to 10 % of full-load) is also

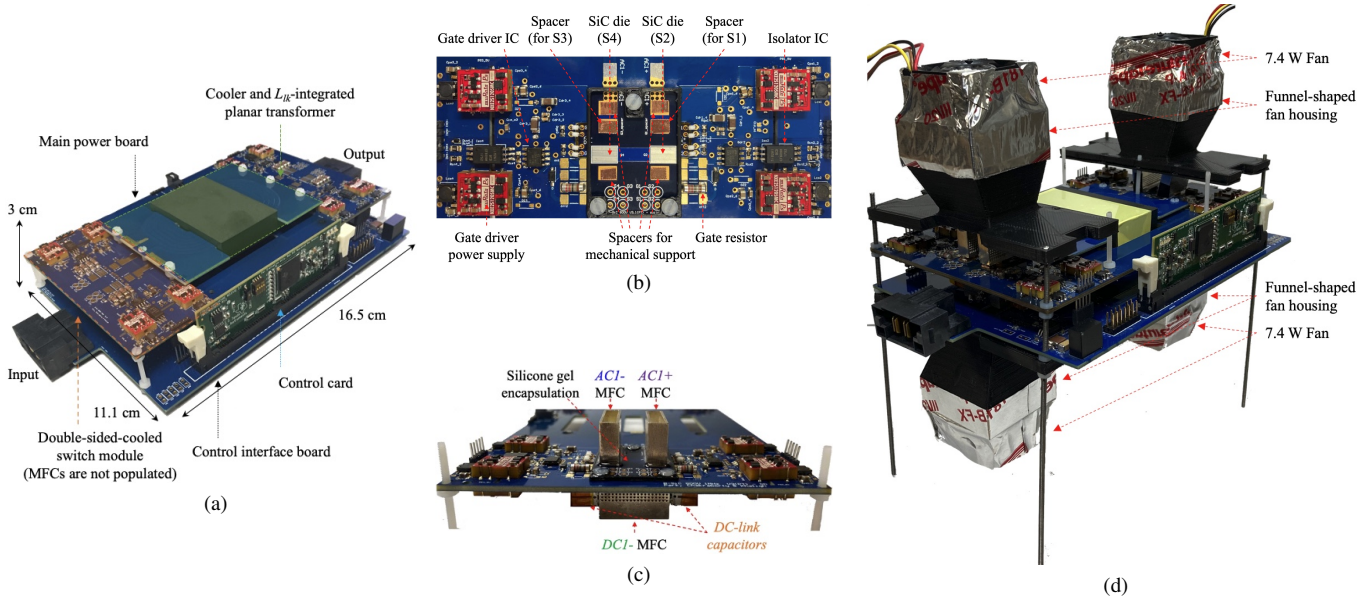

Fig. 15: Photographs of the hardware prototype: (a) Prototype assembly. Switches and MFCs are not populated. The overall height of 3 cm is the height of two MFCs. (b) Detailed view of one full-bridge switch module with bare-die switches and spacers populated on the board. (c) Front view of the main power board with MFCs and silicone gel applied. (d) Temporary assembly for proof-of-concept with housings and fans mounted vertically, directly on the MFCs.

analyzed. As discussed earlier, due to operation with very high switching frequency, realizing ZVS turn-on is crucial in order to achieve reasonably high efficiency over the load range. Since the nominal dc bus voltage V_1 is the same as the maximum battery voltage V_2 (= 380 V), SPS modulation with $D_\phi < 0.25$ (i.e.$< 90°$) is considered first as common DAB design guidelines [39] stipulate the use of SPS for unity voltage-gain condition in order to achieve ZVS with lowest I_{rms}. Trajectories of the modulation parameters and I_{rms} over the load range for this scheme are shown in Fig. 14a, in which the shaded orange zone corresponds to the load range where one or more of the ZVS energy conditions of Table V are missed. The plot illustrates that despite the unity voltage-gain condition, SPS with $D_\phi < 0.25$ is unable to maintain ZVS over most of the partial power range. This is because conventional DAB analyses typically ignore the energy constraint for ZVS (sufficiency condition), instead focusing only on the current-direction constraint (necessary condition) [39]. For completeness, TPS modulation for $D_\phi < 0.25$ with ZVS constraints and a minimum I_{rms} objective function is also analyzed but is found to yield identical results as SPS.

An alternative approach to force ZVS is analyzed next, in which the converter is operated with $D_\phi > 0.25$. Values of the modulation parameters and I_{rms} with this scheme for both SPS and TPS (for minimum I_{rms}) are shown in Fig. 14b. While ZVS is ensured in both cases due to the relatively higher values of current at the switching instants, the RMS current values are significantly higher (than the $D_\phi < 0.25$ case), especially for SPS.

To address the limitations of the previous two approaches, variable control of the dc bus voltage V_1 over the CV range is explored. Operation with variable dc bus voltage in two-stage OBCs has been proposed in some recent works to either improve efficiency [40], [41] or enable operation of universal chargers with wide battery voltage compatibility [42], [43]. In the present work, variable dc bus voltage control is used in conjunction with TPS for $D_\phi < 0.25$ in order to achieve ZVS with the lowest possible I_{rms}. Optimal values of the modulation parameters and V_1 are plotted in Fig. 14c, which shows the wide variation in V_1[4] and the reduction in I_{rms} compared to the TPS case of Fig. 14b, especially at light loads. Further, the non-unity voltage-gain arising from such operation results in triangular waveshape of the transformer current at light loads, which is beneficial in achieving ZVS. Additionally, the energy required for ZVS transitions of the switches of the sending-end bridge at light loads is also lowered due to reduction in both V_1 and $Q_{oss}(V_1)$ (cf. Table V).

IV. Experimental Results

A. Prototype Converter

In order to validate the design and operation of the converter, a proof-of-concept laboratory prototype has been fabricated and tested up to 3.3 kW. Various images of the experimental hardware are shown in Fig. 15 and detailed specifications of the components used in the prototype are listed in Table VI. The converter assembly consists of four different parts: main power PCB, control interface PCB, planar transformer with PCB-based windings and a control card. The power PCB houses the double-sided-cooled, bare-die-based switch modules and the gate-driver circuitries, featuring high-current gate-drivers and power supplies with low isolation capacitance (2.1 pF). Turn-off gate-drive voltage of -5 V is used for improving noise immunity while a turn-on voltage of +15 V is used, since it represents good trade-off for balancing gate-driving losses and switch conduction losses. To be specific, turn-on voltage of +15 V instead of +20 V reduces the gate driving loss from 2 W to 1.25 W (by limiting the

[4] V_1 varies between 170 V - 380 V, which can be accounted for in 230 V ac systems by using a buck-boost type ac-dc PFC stage [42], [43].

TABLE VI
SPECIFICATIONS OF COMPONENTS USED IN THE PROTOTYPE.

Item	Part number or specification	Description
Switch used	CPM2-1200-0025B*	$V_{ds,max}$ = 1200 V, I_D = 98 A, $R_{ds,on}$ = 25 mΩ
DC-link capacitor	B58035U9504M062	V_{rated} = 900 V, $C_{nominal}$ = 0.5 μF
Gate driver power supply	NXE2S1215MC	12 V - 15 V, 2 W, $C_{isolation}$ = 2.1 pF
	NXE2S1205MC	12 V - 5 V, 2 W, $C_{isolation}$ = 2.1 pF
Gate driver IC	IXDN614SI	4.5 V $\leq$ Vcc $\leq$ 35 V, $I_{out,peak}$ = 14 A
Gate resistor	MMB0207 series	1 W MELF resistor
Control card	TMS320F28335	32-bit, 150 MHz MCU
Cooler for switch	-	22×6×15 mm^3 heat-sink made with silver
Fan	9GA0312P3K001	P_{max} = 7.4 W
Silicone gel	915-HT	Dielectric strength > 23 kV/mm
Transformer core	Planar E58/11/38	Material: 3C95
Transformer windings	7-turns in single-layer PCB	Winding thickness: 6 oz (≈ 0.2 mm)

* Lower voltage bare-die switches were not available at component selection stage.

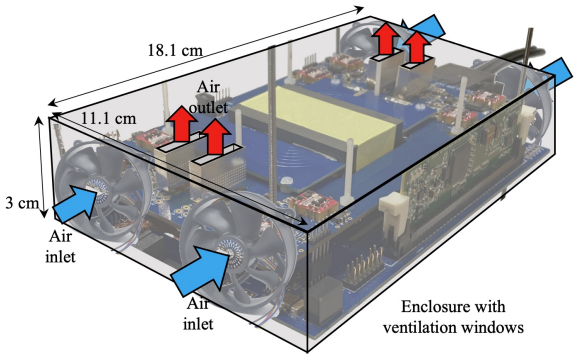

Fig. 16: Projected final converter assembly with enclosure.

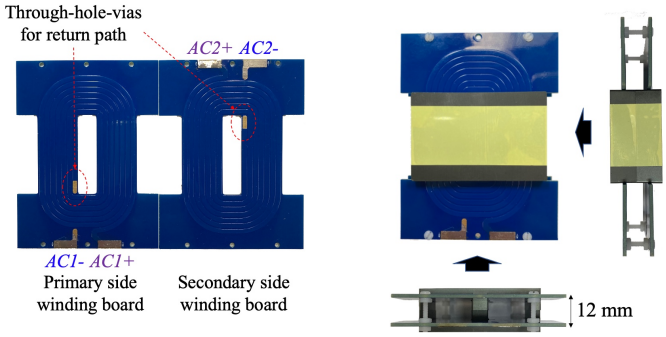

Fig. 17: Transformer board used for experiments: (a) Winding boards for primary and secondary sides. Each board has 7 turns in a single-layer. (b) Complete assembly with the E58/11/38 core in various views.

swing of gate-drive voltage), while the corresponding increase in $R_{ds,on}$ (by about 6 mΩ) increases conduction loss of each switch from 2.95 W to 3.5 W (under the worst conduction loss operating point). Thus, while overall losses remain the same for both +15 V and +20 V, the former allows selection of lower-power-rated gate-driver power supplies with less thermal burden. The turn-on and turn-off gate resistances are 4.7 Ω and 0.89 Ω (two diode-connected 2.2 Ω resistors in parallel with the turn-on resistor). Zoomed-in images of the switch module section are presented in Fig.15b, 15c, which show the bare-dies, spacers and other important components. It is worth noting that silicone gel is applied to encapsulate the bare-dies, as seen in Fig. 15c. This helps enhance the long-term reliability of the module by improving electrical isolation and also protects the dies from moisture, chemicals and contaminants [44].

In the prototype hardware, the MFCs are directly soldered to the dies and the spacers. However, since the MFCs are relatively large compared to the dies and protruded, external shocks or vibrations from outside can be transferred to the dies through the MFCs, which can impact the mechanical stability of the switch module. In order to address this, additional floating pads and spacers are populated beside the spacers for the source connections, as shown in Fig. 15b. These additional spacers are also soldered to the corresponding MFCs to provide additional mechanical support and lessen mechanical stress on the MOSFET dies by distributing the force. The switches in the prototype are forced-air-cooled using a fan mounted on a pair of adjacent MFCs through a fan housing, as shown in Fig. 15d. The fan housing also functions as an auxiliary mechanical fixture for the MFCs by holding the parts in place. A rubber band is used for the joint between the MFCs and the housing to avoid excessive or unevenly distributed force on the dies. This band can also serve as a gasket for cooling fluids. If it is desired to improve the mechanical stability further, pressure contacts or spring contacts can be considered for the connection of the MFCs. For example, the use of "Fuzz-button" [45], which is a flexible press pin, with a low-profile interposer can be considered for the proposed switch module also.

Overall dimensions of the assembly depicted in Fig. 15a correspond to an overall volume of 549.45 cm^3 and a power density of 6 kW/L. This includes the main power PCB, control interface PCB, control card and MFCs on the power PCB (not populated in Fig. 15a). However, it should be noted that the fans are not included in the prior volume estimation. As seen by Fig. 15d, the fans with associated housings increase the Z-dimension significantly in comparison to Fig. 15a. However, this arrangement is only for the proof-of-concept prototype. In a final prototype, the funnel-shaped fan housing will be absent and the assembly will be surrounded by an enclosure having ventilation windows, with suitably-selected fans fitted horizontally at its sides, as illustrated in Fig. 16. In the final converter, the enclosure would also act as the auxiliary mechanical fixture to lessen the force transferred to the SiC dies. With this modification, the x-dimension of the prototype is estimated to increase to 18.1 cm (compared to 16.5 cm in Fig. 15a), and the power-density of the complete assembly (including fans) is projected to be 5.44 kW/L.

As shown in Fig. 17, for the transformer, E58/11/38-3C95 cores with two 7-turn, single-layer PCBs were used with a copper thickness of 6 oz (≈ 0.2 mm). In order to obtain

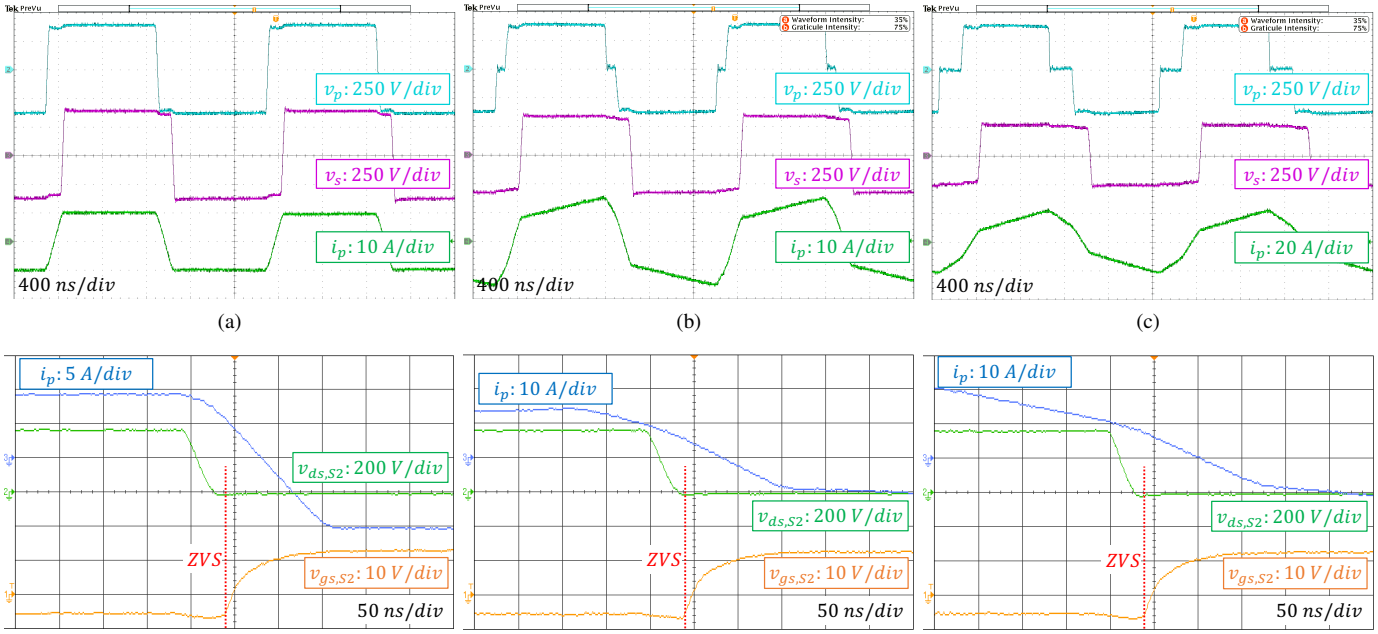

Fig. 18: Key waveforms in the CP zone with output power (P_{out}) fixed at 3.3 kW. Transformer voltages and current for (a) $V_2 = 380$ V, (b) $V_2 = 320$ V and (c) $V_2 = 250$ V. ZVS waveforms of one switch in the sending-end bridge for (d) $V_2 = 380$ V, (e) $V_2 = 320$ V and (f) $V_2 = 250$ V.

the desired leakage inductance (4.8 μH), the gap between the primary-side and secondary-side windings is set to be 12 mm. The inductance can be easily adjusted by changing the gap between the primary and secondary side windings [37]. The leakage inductance of the transformer and ac resistance of each winding at 500 kHz are measured using a Keysight E4990A impedance analyzer and were found to be 4.9 μH and 0.1 Ω respectively, which show a very close agreement with corresponding theoretically predicted values in Section III-B.

B. Power Test

Fig. 18 shows key waveforms of the DAB converter at V_1 = 380 V, based on the target CP charging stage, as per which the battery voltage is charged from 250 V to 380 V at a constant power of 3.3 kW. The tests are conducted in open-loop with a fixed switching frequency of 500 kHz and a Chroma 63206A electronic load is used for emulating the battery port. Following the optimization results in Fig. 9, SPS is implemented for high V_2 ($>$ 360 V), and DPS with inner phase-shift on the primary-side bridge is used for low V_2 ($<$ 360 V) as they ensure minimum RMS current operation while achieving ZVS of all switches. As can be observed from the transformer voltages and current waveforms in Fig. 18a-18c, no significant oscillation is present, which indicates that the parasitics of the switch module and transformer are sufficiently low, as targeted. Fig. 18d-18f show the drain-source voltage and gate-source voltage of S_2, which is in the leg that has the most stringent condition in terms of ZVS. The waveforms demonstrate that ZVS is achieved over the all operating conditions.

Thermal images taken using an infrared (IR) thermal imaging camera (FLIR E6) at the highest power (3.3 kW) operating

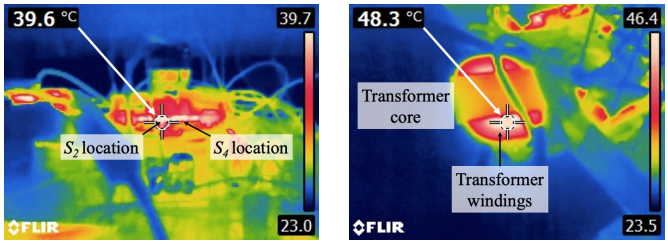

Fig. 19: IR images of the converter at 3.3 kW operation: (a) Front view of the switch module part under forced-air condition, highlighting the locations of the switches. (b) Top view of the transformer. The maximum temperatures of the switch and the windings are around, respectively, 39.6°C and 48.3°C at an ambient temperature of 23.5°C.

condition are shown in Fig. 19, from which it can be observed that the overall temperature anywhere in the converter does not exceed 50°C when the ambient temperature (T_{amb}) is around 23°C. Specifically, the maximum temperature measured at the location of the switch die was around 40°C, indicating a temperature rise of around 17°C above ambient. As discussed in section II-B, detailed thermal studies done in [31] indicate that the junction to ambient thermal resistance ($R_{\theta,j-a}$) is around 1.9 °C/W for the switch module, which is at par or better than most forced-air cooled solutions. For the transformer, the maximum temperature of the windings was around 48°C, while the core temperature was even lower (benefiting from the planar structure's large, exposed surface area). In summary, the results indicate that the converter's thermal performance is quite satisfactory for the test conditions (T_{amb} = 23°C) with maximum temperature rise of 17°C and 25°C above ambient for the switch part and transformer respectively. For practical OBCs inside vehicles, where ambient temperature is

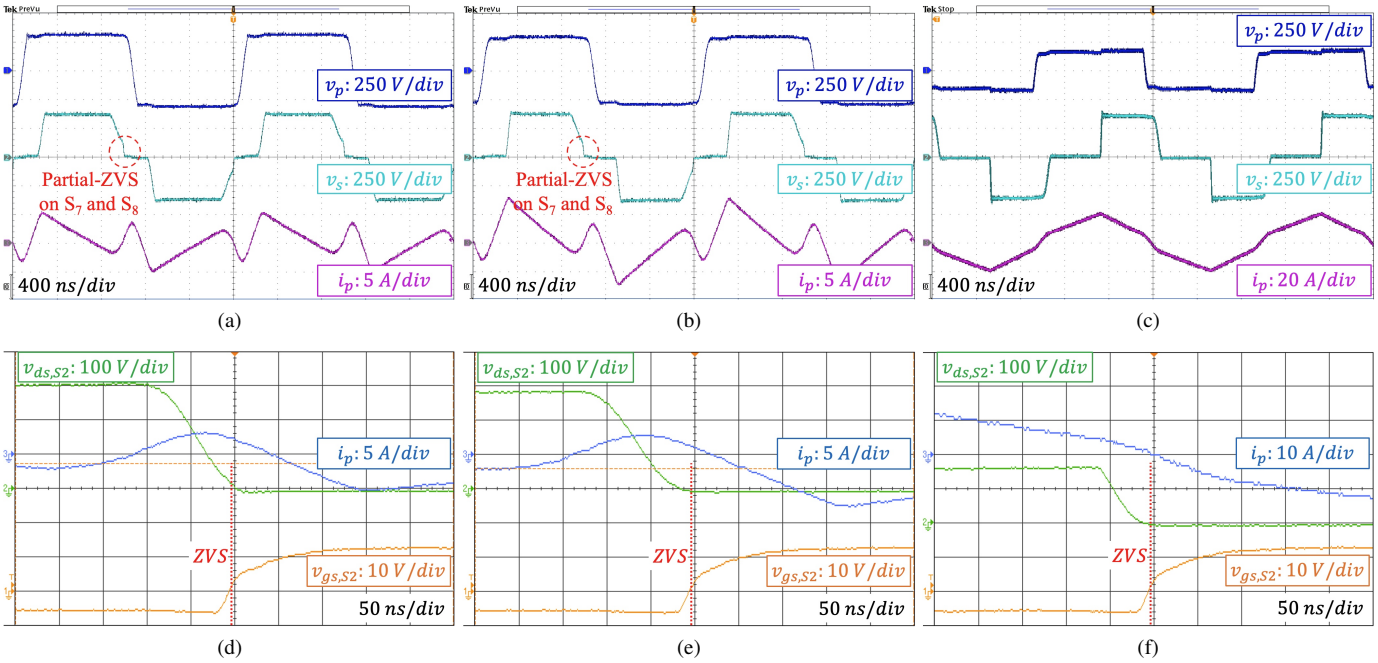

Fig. 20: Key waveforms in the CV zone with battery voltage (V_2) fixed at 380 V. Transformer voltages and current for (a) $P_{out} = 330$ W (10% load) with $V_1 = 310$ V, (b) $P_{out} = 550$ W (16.7% load) with $V_1 = 290$ V and (c) $P_{out} = 1850$ W (55% load) with $V_1 = 170$ V. ZVS waveforms of one switch in the sending-end bridge for (d) $P_{out} = 330$ W, (e) $P_{out} = 550$ W and (f) $P_{out} = 1850$ W.

higher and typically around 60°C, if similar temperature rises are assumed, the maximum temperature of the switches and transformer can be projected to be around 80°C and 85°C respectively, indicating a thermally feasible design for OBC systems. Further enhancement of the cooling performance is possible using liquid-cooling for the switches and the transformer, which are discussed in detail in [30] and [31] respectively.

Fig. 20 shows experimental results of important waveforms under the light-load conditions of the CV stage. As discussed in section III-D, the additional modulation of V_1 is implemented for operation at light-load conditions to achieve ZVS utilizing the triangular waveshape of i_p. The results demonstrate that most switches achieve full-ZVS even under harsh conditions for the DAB topology. However, as highlighted in Fig. 20a and 20b, the fourth half-bridge consisting of S_7 and S_8 shows slightly partial ZVS at such low powers ($P_{out} < 600$ W) unlike the expectation. As discussed in [46], this can be due to the non-idealities in the real operation, including finite slew-rate and non-negligible skew of the drain-source voltages. Except for this discrepancy, the key voltage and current waveforms of the converter show good adherence with theoretical predictions, which indicates that the converter operates well under light load conditions.

Fig. 21 shows the experimental efficiency of the prototype converter on a typical CP-CV charging profile of EV Li-ion battery, measured using a Tektronix PA3000 power analyzer. The results demonstrate that the converter can operate with consistently high efficiency (95.8 - 98%) during the CP charging stage, under high switching frequency (500 kHz). This can be attributed to the optimal design of the integrated transformer that enables to achieve minimized RMS current and full-ZVS

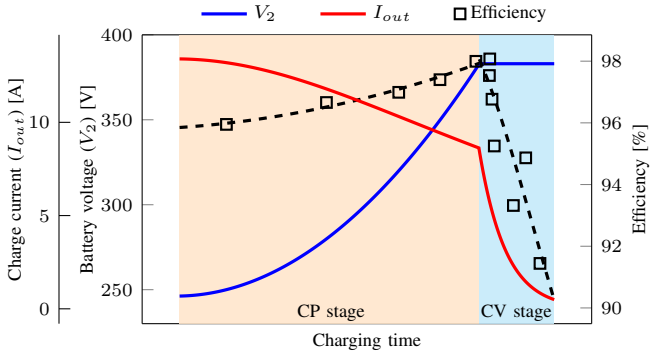

Fig. 21: Measured efficiencies of the prototype converter on a typical CP-CV charging profile for an EV Li-ion battery [38]. The dashed lines show a corresponding best-fit trend-line. CP stage and CV stage are highlighted by orange and blue zones, respectively. Control and gate-driver losses are excluded in the efficiency measurement.

operation over the entire output voltage range. Focusing on the CP stage operation, the efficiency keeps increasing as the output voltage increases. This tendency is in accordance with the observation in Fig. 11, where the overall losses decrease as V_2 increases due to the RMS current-related losses ($P_{windings}$ and P_{sw}) are dominant at V_2 values lower than 380 V. The efficiencies at light-load conditions are also measured over the wide load range from 330 W (10% of the full-load) to 3.3 kW. Additional dc-bus voltage modulation is implemented as discussed in Section III-D, and the results show reasonably high efficiency values. As discussed, it can be inferred that the efficiencies can be further enhanced if the partial ZVS turn-on phenomenon at very low powers is resolved by using improved analytical modeling [46] for obtaining more realistic modulation parameters.

TABLE VII
COMPARISON OF THE PROTOTYPE CONVERTER WITH RECENTLY-PROPOSED DC-DC CONVERTERS FOR 3.3 KW OBC SYSTEMS.

Reference	[7]	[4]	[6]	[47]	[48]	This work
Topology	Hybrid LLC	LLC	CLLC	Series resonant	CLLC	DAB
Charging profile	CC-CV	CP	CC-CV	CP	CP	CP-CV
Switch type	GaN	Si	GaN	Si	GaN	SiC
f_s [kHz]	75-300	48-86	900-1250	150-190	100	500
Power-density [kW/L]	4	$<4^{*}$	9.22^{**}	1	3.14^{*}	5.44
Peak efficiency at 3.3 kW [%]	98.5	97.6	96	98.1	98.25	98

* Value is estimated from photograph of the prototype.
** Value does not include cooling components and microcontroller.

The designed converter is compared with several recently presented works, developed for the same 3.3 kW OBC applications, and the comparison results are listed in Table VII. As shown, at comparable conversion efficiency, the proposed converter demonstrates relatively high power-density, including all required components such as microcontroller circuitry and fans. It might be noted that the selected switch (CPM2-1200-0025B) has far higher voltage rating (1200 V) than the voltage level (<400 V) of the designed converter. This over-design was due to the non-availability of lower voltage-rated bare-die SiC devices at the component selection stage. Thus, in future design iterations use of more appropriately selected lower voltage-rated (e.g., 650 V) devices can be one way to enhance efficiency as $R_{ds,on}$ of a MOSFET varies inversely with its blocking voltage.

V. Conclusions

This paper has presented detailed electrical design methodology of a highly compact and efficient 3.3 kW, 500 kHz DAB converter for the dc-dc stage of OBC systems, operated with CP charging. The use of a wire-bondless, bare-die SiC MOSFET-based full-bridge module with small form-factor, integrated cooling systems is one of the key drivers which helps enhance power-density and efficiency. The low parasitics of the developed switch module enables the converter to operate at high frequency without exhibiting high switching losses and oscillations. Integration of the DAB inductor as the leakage inductance of a planar transformer is the other key strategy, enabling a compact design. Optimal design of the transformer parameters is discussed in detail, which ensures ZVS across the target battery voltage range (250 V-380 V) while maximizing average efficiency. The optimization is conducted based on accurate analytical modeling of the converter operation and comprehensive study on the correlation between the transformer design domain and the operation of the converter. Performance evaluation of the proposed converter is conducted on a laboratory prototype, which is operated up to 3.3 kW and has a final projected power-density of 5.44 kW/L. Experimental results demonstrate good-quality high-frequency waveforms with ZVS and consistently high conversion efficiency (95.8-98%) over the CP charging stage, as targeted. Also, reasonably high efficiencies at light-load conditions are validated. Future work will explore detailed characterization of the switch module and increasing the power level of the converter using forced-cooling for the transformer.

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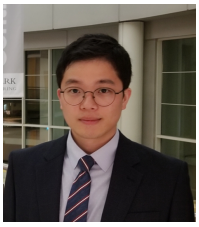

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